Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

HP 16710A, HP 16711A, and HP 16712A 100-MHz State/ 500-MHz Timing Logic Analyzer

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The HP 16710A, HP 16711A, and HP 16712A are 100-MHz State/500-MHz Timing Logic Analyzer modules for the HP 16600- and HP 16700-series Logic Analysis Systems. These modules offer high performance measurement capability.

Features

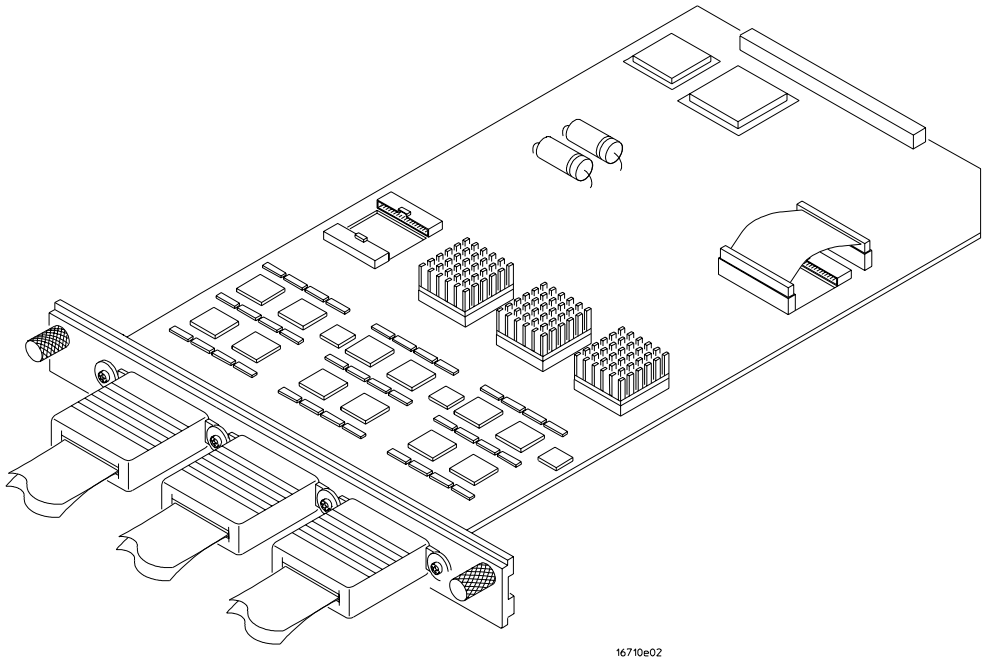
Some of the main features of the HP 16710A/11A/12A are as follows:

- 96 data channels
- 6 clock/data channels
- 8K memory depth per channel (HP 16710A)
  32K memory depth per channel (HP 16711A)
  128K memory depth per channel (HP 16712A)
- 100-MHz maximum state acquisition speed
- 500-MHz maximum timing acquisition speed
- Expandable to 204 channels

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the logic analyzer module.

This module can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.



The HP 16710A/11A/12A Logic Analyzer

In This Book

This book is the service guide for the HP 16710A/11A/12A 140-MHz State/ 500-MHz Timing Logic Analyzer module. Place this service guide in the 3-ring binder supplied with your HP 16600- or HP 16700-series Logic Analysis System Service Manual.

This service guide is divided into eight chapters.

Chapter 1 contains information about the module and includes accessories for the module, specifications and characteristics of the module, and a list of the equipment required for servicing the module.

Chapter 2 tells how to prepare the module for use.

Chapter 3 gives instructions on how to test the performance of the module.

Chapter 4 contains calibration instructions for the module.

Chapter 5 contains self-tests and flowcharts for troubleshooting the module.

Chapter 6 tells how to replace the module and assemblies of the module and how to return them to Hewlett-Packard.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the analyzer works and what the self-tests are checking.

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HP 16710A/11A/12A 100-MHz State/500-MHz Timing Logic Analyzer

5 Troubleshooting

6 Replacing Assemblies

7 Replaceable Parts

8 Theory of Operation

1

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the HP 16710A/11A/12A Logic Analyzer.

Accessories Supplied	HP Part Number
Probe Tip Assembly, Qty 6	01650-61608
Grabbers, Qty 6 packages	5090-4356
Extra Probe Leads, Qty 1 package	5959-9333
Extra Probe Grounds, Qty 6 packages	5959-9334
Probe Cable and Pod Labels, Qty 1	01650-94312
Double Probe Adapter, Qty 1	16542-61607
Master/Expander Interconnect Cable	16555-61601

Mainframe and Operating System

The HP 16710A/11A/12A Logic Analyzer requires an HP 16600- or HP 16700-series logic analysis system with operating system version A.01.20.00 or higher.

The HP 16600-series logic analysis system supports a single-card HP 16710A/11A/12A. The HP 16700-series logic analysis system supports a one- or two-card HP 16710A/11A/12A module. With five slots, the HP 16700-series logic analysis system can support two two-card modules and a one-card module.

Specifications

The specifications are the performance standards against which the product is tested.

Threshold Accuracy	± (100 mV + 3% of threshold setting)
Maximum State Speed	100 MHz
Minimum Master-to-Master Clock Time *	10.000 ns

Setup/Hold Time for Different Clock Schemes: *

Single Clock, Single Edge:	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges:	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges:	0.0/5.0 ns through 5.0/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = -0.9 V, VL = -1.7 V, and threshold = -1.3 V.

Environmental Characteristics

Probes

Maximum Input Voltage	± 40 V, CAT I

Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable.

Operating Power

Supplied by mainframe

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 95% relative humidity at +40 °C (+122 °F).
Altitude	To 4600 m (15,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	100 MHz, 4.0 ns pulse width, < 600 ps rise time	HP 8133A Option 003	P, T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A mainframe with HP 54751A plug-in module	P
Function Generator	Accuracy $\leq(5)(10^{-6}) \times$ frequency, DC offset voltage ±1.5 V	HP 3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A	P
BNC-Banana Cable		HP 11001-60001	P
BNC Tee	BNC (m)(f)(f)	HP 1250-0781	P
SMA Coax Cable (Qty 3)	≥ 18 GHz bandwidth	HP 8120-4948	P
BNC Coax Cable	BNC (m-m), > 2 GHz bandwidth	HP 8120-1840	P
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200	P
Adapter	SMA(f)-BNC(m)	HP 1250-2015	P
Coupler	BNC (m-m)	HP 1250-0216	P
20:1 Probes (Qty 2)		HP 54006A	P
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P, T

A = Adjustment, P = Performance Tests, T = Troubleshooting

**Instructions for making these test connectors are in chapter 3, “Testing Performance.”

2

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed in chapter 1. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20 °C to +35 °C (+68 °F to +95 °F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C (-40 °F to +167 °F)
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

Accessories supplied with the module are listed in chapter 1, "Accessories Supplied."

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Hewlett-Packard Sales Office. Arrangements for repair or replacement are made, at Hewlett-Packard's option, without waiting for a claim settlement.

To prepare the mainframe

CAUTION Turn off the mainframe power before removing, replacing, or installing the module.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Remove power from the instrument.

- **a** Exit all logic analysis sessions. In the session manager, select Shutdown.
- **b** At the query, select Power Down.
- **c** When the "OK to power down" message appears, turn the instrument off.
- **d** Disconnect the power cord.
- **e** Disconnect any input or output connections.

2 Plan your module configuration.

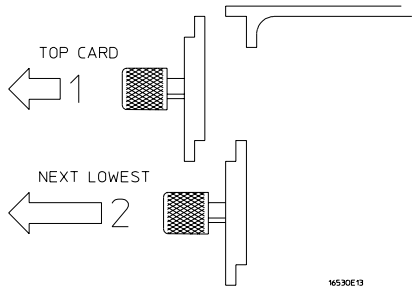
If you are installing a one-card module, use any available slot in the mainframe.

If you are installing a multi-card module, use adjacent slots in the mainframe.

3 Loosen the thumb screws.

Cards or filler panels below the slots intended for installation do not have to be removed.

Starting from the top, loosen the thumb screws on filler panels and cards that need to be moved.



4 Starting from the top, pull the cards and filler panels that need to be moved halfway out.

CAUTION All multi-card modules will be cabled together. Pull these cards out together.

5 Remove the cards and filler panels.

Remove the cards or filler panels that are in the slots intended for the module installation. Push all other cards into the card cage, but not completely in. This is to get them out of the way for installing the module.

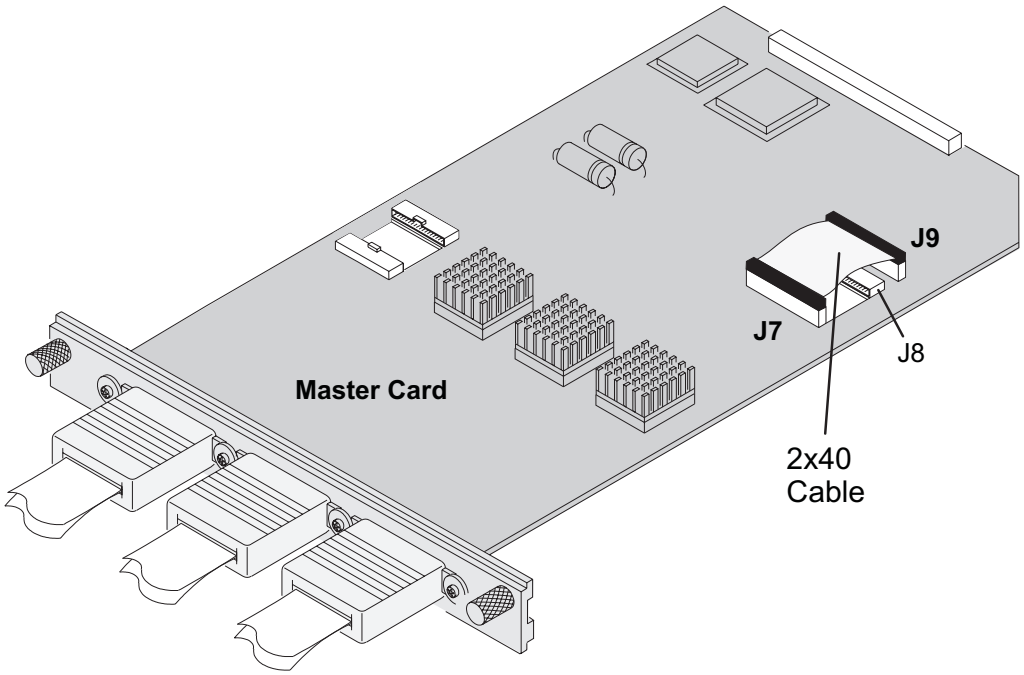
Some modules for the logic analysis system require calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.

To configure a one-card module

- When shipped separately, the module is configured as a one-card module. The cables should be connected as shown in the figure.
- To configure a two-card module into one-card modules, remove the cables connecting the two cards, then connect the cables as shown (see figure below).

CAUTION If you pull on the flexible ribbon part of the cable, you might damage the cable assembly. To remove a cable from the cable connector on the board, use a screwdriver to gently pry the hard plastic part of the cable assembly away from the connector.

NOTE Directions for connecting the cables are printed on the circuit board.



To configure a two-card module

NOTE Directions for connecting the cables are printed on the circuit board.

To configure a two-card module, connect the cables as follows.

1 Disconnect the 2x40 cable from J7 and J9 of the lower card.

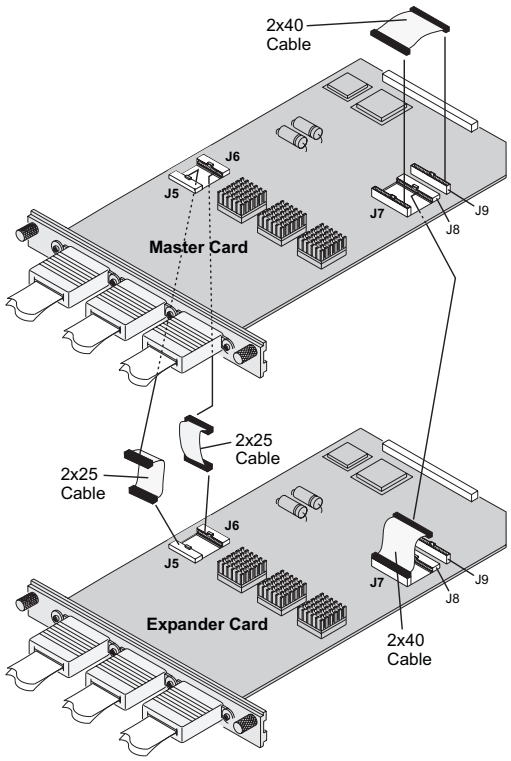
CAUTION If you pull on the flexible ribbon part of the cable, you might damage the cable assembly. To remove a cable from the cable connector on the board, use a screwdriver to gently pry the hard plastic part of the cable assembly away from the connector.

2 Connect the 2x25 cable from J5 of the lower card to J5 of the upper card. Connect the 2x25 cable from J6 of the lower card to J6 of the upper card.

3 Connect the 2x40 cable from J7 of the lower card to J8 of the upper card.

You might have to remove one end of the 2x40 cable on the upper card to access the J8 connector. When finished, ensure that the 2x40 cable connecting J7 and J9 on the upper card is firmly seated.

NOTE Save unused cables for future configurations..

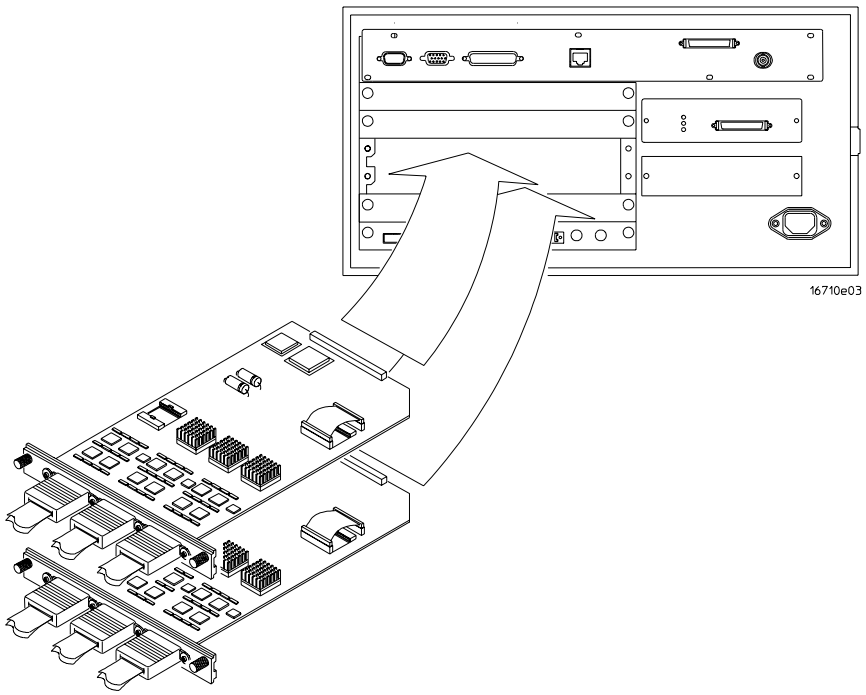


NOTE The upper card is the Master Card.

To install the module

1 Slide the cards above the slots for the module about halfway out of the mainframe.

2 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



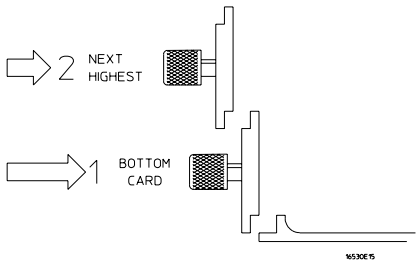
3 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 5.

4 Position all cards and filler panels so that the endplates overlap.

5 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.



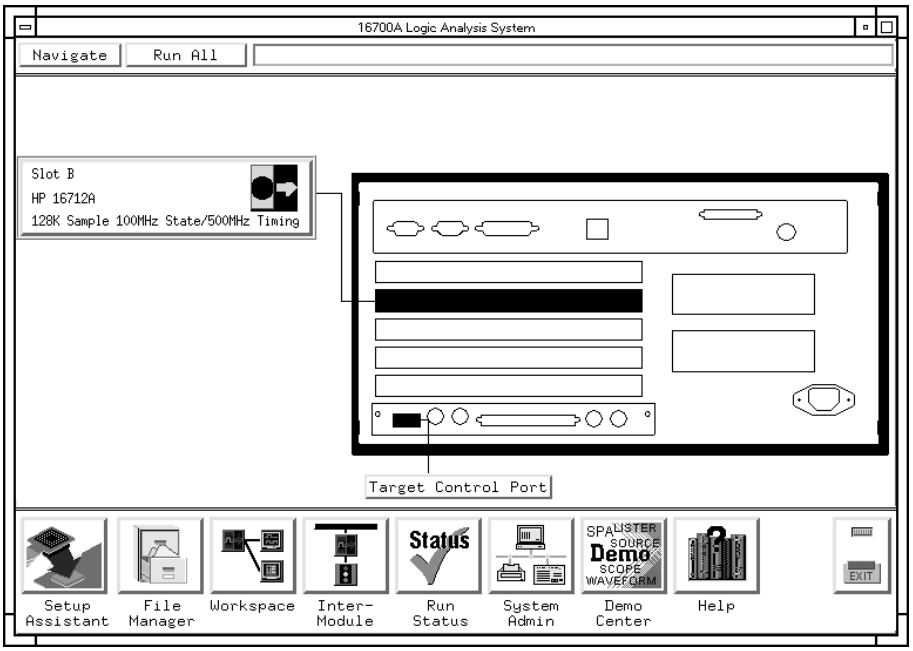
CAUTION Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To turn on the system

1 Connect the power cable to the mainframe.

2 Turn on the instrument power switch.

When you turn on the instrument power switch, the instrument performs powerup tests that check mainframe circuitry. After the powerup tests are complete, the screen will look similar to the sample screen below.



To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the module does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a “Pass” status for each of the tests.

Test Strategy

This chapter shows the module being tested in an HP 16700A-series mainframe. A one-card module can also be tested in an HP 16600A-series mainframe.

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test.

One-Card Module. To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Two-card Module. To perform a complete test on a two-card module, perform the self-tests with the cards connected. Then, remove the two-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the one-card manual performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into a two-card module, reinstall it into the mainframe and perform the final two-card test. For removal instructions, see Chapter 6, “Replacing Assemblies.” For installation and configuration instructions, see Chapter 2, “Preparing for Use.”

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

To Perform the Self-tests

There are two types of self-tests: self-tests that automatically run at power-up, and self-tests that you select on the screen. The self-tests verify the correct operation of the logic analysis system. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

Perform the power-up tests

The logic analysis system automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self Tests. Tests that are performed during power-up are not repeated in the Self Tests.

The monitor, keyboard and mouse must be connected to the mainframe to observe the results of the power-up tests.

1. **Disconnect all inputs and exit all logic analysis sessions.**

   In the Session Manager, select **Shutdown**. In the Powerdown window, select **Powerdown**.

2. **When the "OK to power down" message appears, turn off the power switch.**
3. **After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:**

   - ensure all of the installed memory is recognized
   - any error messages
   - interrupt of the boot process with or without error message

   A complete transcript of the boot dialogue is in the HP 16600- or HP 16700-series Logic Analysis System Service Manual, Chapter 8, "Theory of Operation".

4. **During initialization, check for any failures.**

   If an error or an interrupt occurs, refer to the HP 16600- or HP 16700-series Logic Analysis System Service Manual, Chapter 5, "Troubleshooting".

Perform the self-tests

The self-tests verify the correct operation of the logic analysis system and the installed HP 16710A, HP 16711A, or HP 16712A module. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

1 Launch the Self-Tests.

- **a** In the System window, click on System Admin.
- **b** Under the Admin tab, click on Self-Test . . .
- **c** In the query pop-up, select Yes to exit the current session.

  The Self-Test closes down the current session because the test algorithms leave the system in an unknown state. Re-launching a session at the end of the tests will ensure the system is properly initialized.

2 In the Self-Test window select Test All.

When the tests are finished, the Status will change to TEST passed or TEST failed. You can find detailed information about the test results in the Status Message field of the Self-Test window.

The System CPU Board test returns Untested because the CPU tests require user action. To test the CPU Board, select CPU Board, then select each test individually.

3 Select Quit to exit the Test menu.

4 In the Session Manager, select Start Session This Display to re-launch a logic analysis session.

To Make the Test Connectors

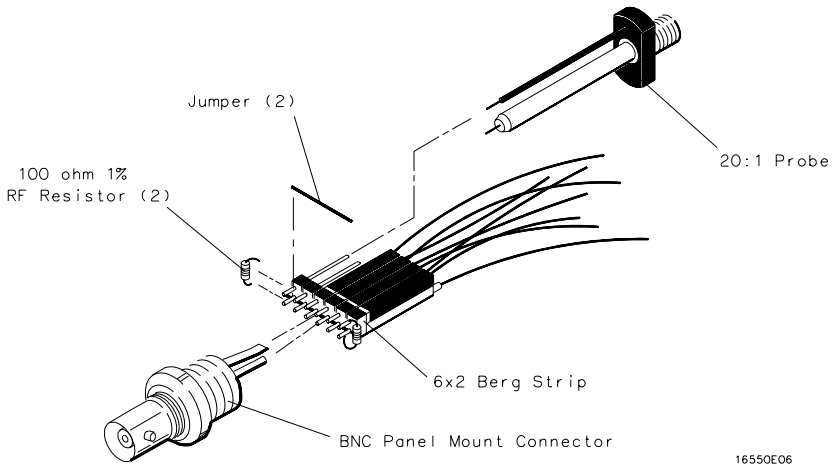
The test connectors connect the logic analysis system to the test equipment.

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	HP 1250-1032	4
100 Ω 1% resistor	HP 0698-7212	6
Berg Strip. 17-by-2		1
Berg Strip, 6-by-2		3
20:1 Probe	HP 54006A	2
Jumper wire		

1 Build three test connectors using BNC connectors and 6-by-2 sections of Berg strip.

- **a** Solder a jumper wire to all pins on one side of the Berg strip.
- **b** Solder a jumper wire to all pins on the other side of the Berg strip.
- **c** Solder two resistors to the Berg strip, one at each end between the end pins.
- **d** Solder the center of the BNC connector to the center pin of one row on the Berg strip.
- **e** Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.
- **f** On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



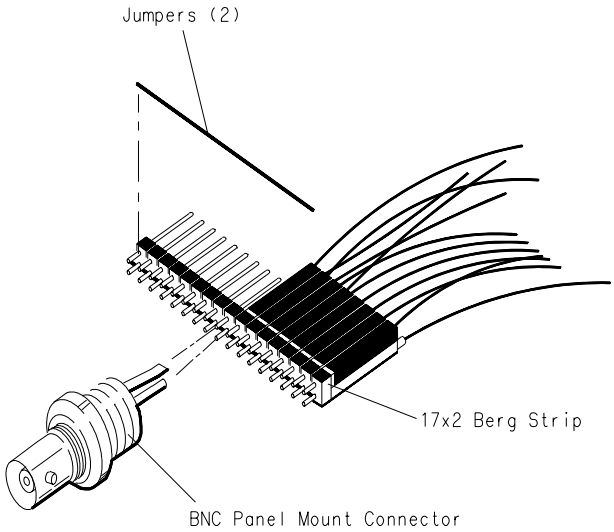
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



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To Set up the Test Equipment and the Analyzer

Before testing the specifications of the HP 16710A/11A/12A logic analyzer, the test equipment and the logic analysis system must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analysis system. Before performing any or all of the following tests in this chapter, the following steps must be followed.

NOTE Multi-card modules must be separated into single-card modules.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A
Function Generator	DC offset voltage ±1.5 V	HP 3325B Option 002

Set up the equipment

1. Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.
2. Turn on the logic analysis system.
   - **a** Connect the keyboard, mouse, and monitor to the rear panel of the logic analysis system mainframe.
   - **b** Plug in the power cord to the power connector on the rear panel of the mainframe.
   - **c** Turn on the main power switch on the mainframe front panel.
3. Set up the logic analysis system.
   - **a** Open the Session Manager window and select “Start Session on This Display”.
   - **b** In the Logic Analysis System window, select Navigate, then select Active Modules, then select Slot n: MACHINE 1 (where “n” is the slot the module under test is installed), then select Setup. A Setup window will now open.
   - **c** In the MACHINE 1 Setup window, select Navigate, then select Slot n: MACHINE 1 (where “n” is the slot the module under test is installed), then select Listing. A Listing window will open.
   - **d** In the MACHINE 1 Setup window, select the Config tab.
4. Set up the pulse generator according to the following table.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 10.000 ns	Mode: Pulse Divide: Pulse ÷ 2 Width: 4.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)

5 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule graphs: 2	Level: 0.0 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	Thresholds: user-defined Units: Volts Upper: - 980 mV Middle: -1.30 V Lower: -1.62 V

Allow the logic analysis system to warm up for 30 minutes before beginning any of the following tests.

To Test the Threshold Accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy

These instructions include detailed steps for testing the threshold settings of Pod 1. After testing Pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for Pod 1, substituting the next pod for Pod 1 in the instructions.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A
Function Generator	DC offset voltage ± 1.5 V	HP 3325B Option 002
BNC-Banana Cable		HP 11001-60001
BNC Tee		HP 1250-0781
BNC Cable		HP 8120-1840
BNC Test Connector, 17x2		

Set up the equipment

1 If you have not already done so, perform the procedure described in "To Set up the Test Equipment and the Analyzer" on page 3-7.

2 Set up the function generator.

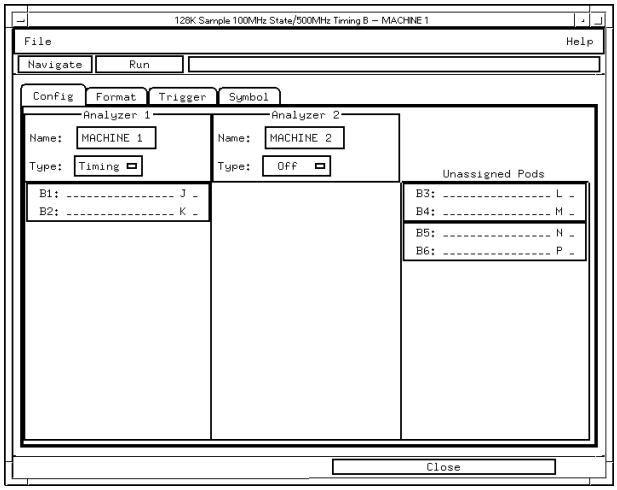
a Set up the function generator to provide a DC offset voltage at the Main Signal output.

b Disable any AC voltage to the function generator output, and enable the high voltage output.

c Monitor the function generator DC output voltage with the multimeter.

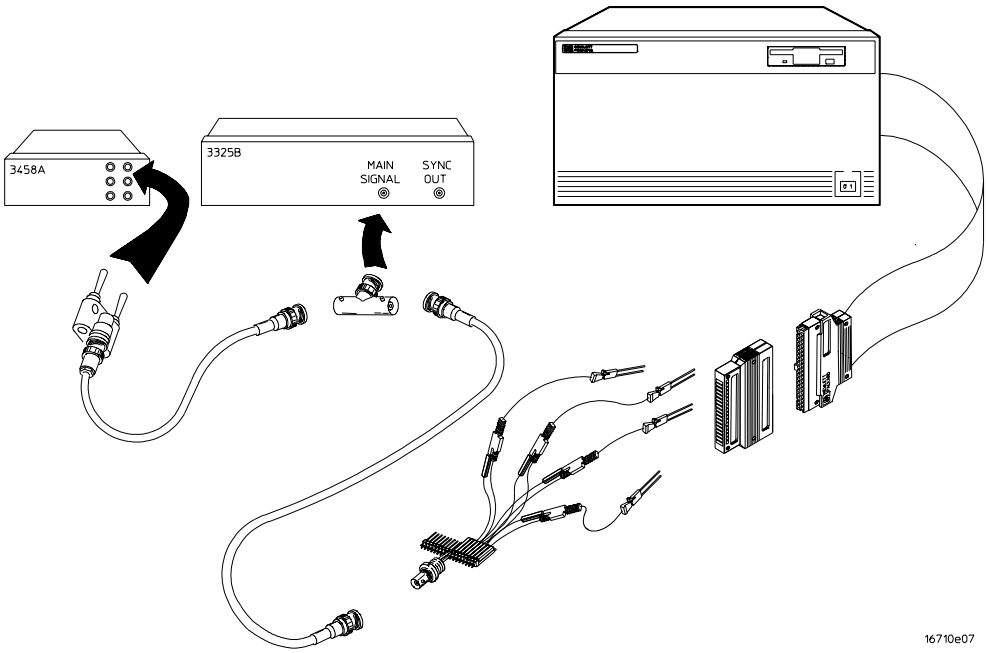
Set up the logic analyzer

1. In the MACHINE 1 Setup window, select the Config tab.
2. Under the Config tab, unassign the pods that are assigned to Analyzer 2. To unassign the pods, use the mouse to drag the pods to the Unassigned Pods column.



Connect the logic analyzer

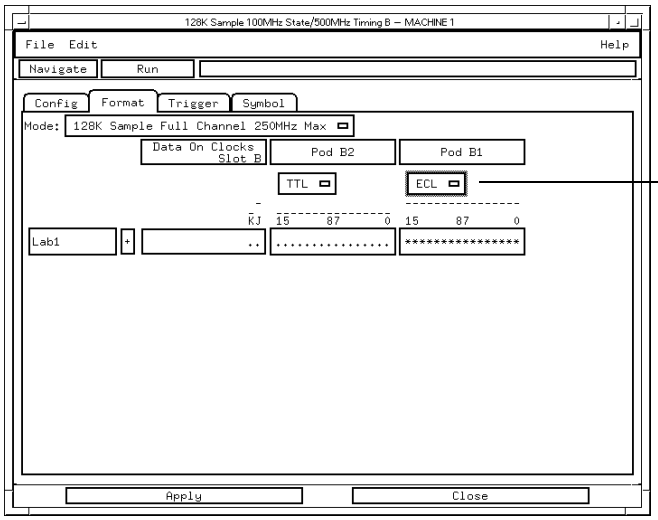
1. Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of Pod 1 to one side of the BNC Tee.
2. Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.
3. Connect the BNC Tee to the Main Signal output of the function generator.



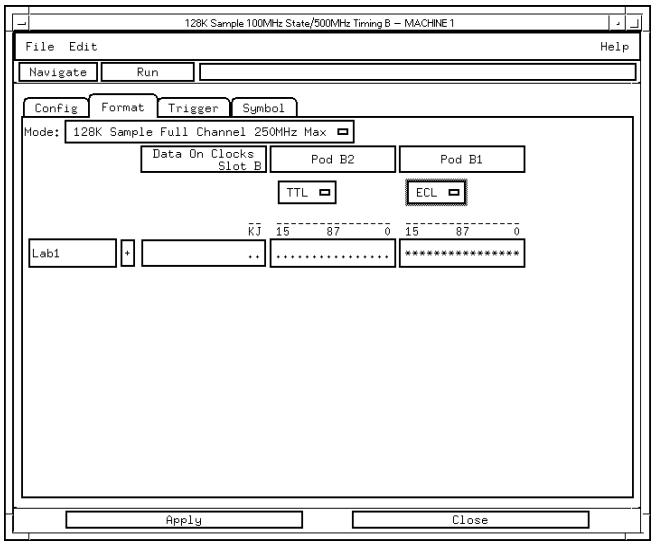
Test the ECL threshold

1. Under the Format tab, select the threshold field for the pod under test, then select ECL.
2. On the function generator front panel, enter -1.159 V ±1 mV DC offset. Use the multimeter to verify the voltage.

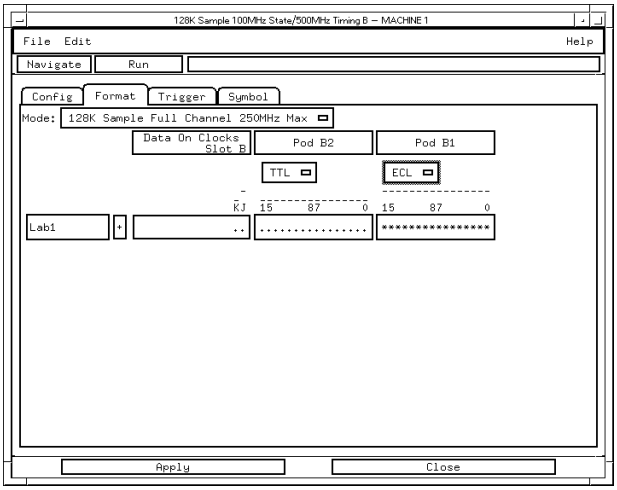
   The activity indicators for Pod 1 should show all data channels and the J-clock channel at a logic high.



3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic low. Record the function generator voltage in the performance test record.



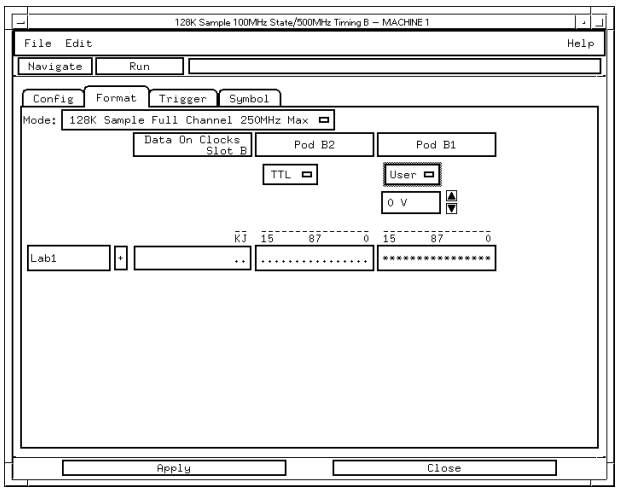
4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic high. Record the function generator voltage in the performance test record.



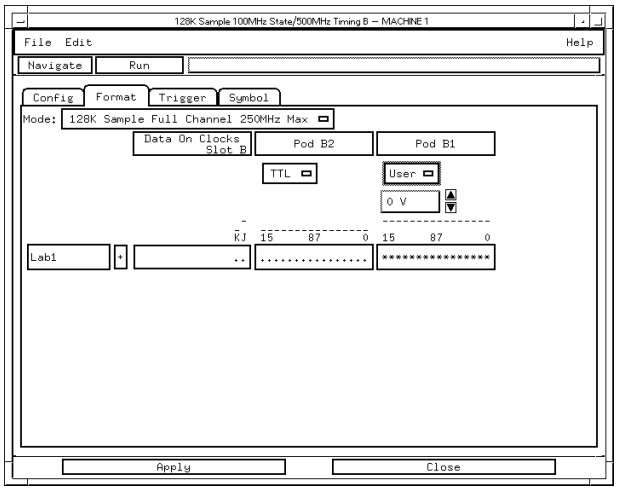
Test the 0 V User threshold

1. Under the Format tab, select the threshold field, then select User. In the numeric field, enter 0 V.
2. On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for the pod under test should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the next pod

Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator as shown in “Connect the logic analyzer” on page 3-11. If you have just finished testing Pod 1, connect the data and clock channels of Pod 2. Repeat until all pods have been tested.

Note that the pod under test must be assigned to the analyzer. For Pod 3, use the MACHINE 1 Setup menu under the Config tab, unassign Pods 1 and 2 and assign Pods 3 and 4 to Analyzer 1. Repeat this unassignment and assignment each time you test an odd-numbered pod.

When you have finished testing the last pod, you have completed the threshold accuracy test.

To Test the Single-clock, Single-edge, State Acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using a single-edge clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler (Qty 3)	BNC (m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 3-7. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

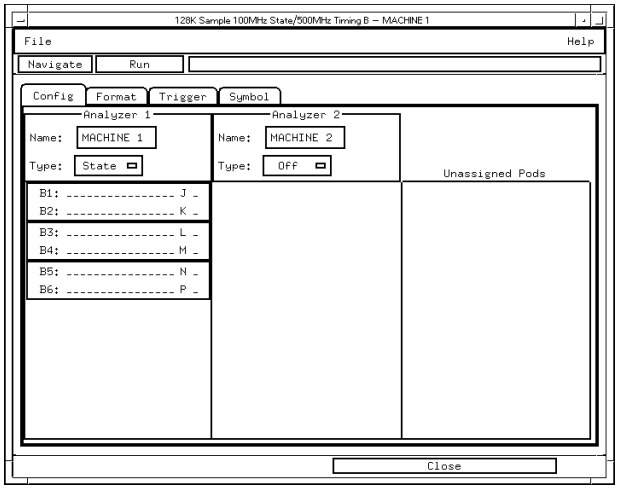
Set up the logic analyzer

1 Set up the Configuration tab.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 Type box select Timing, then in the pop-up menu select State.

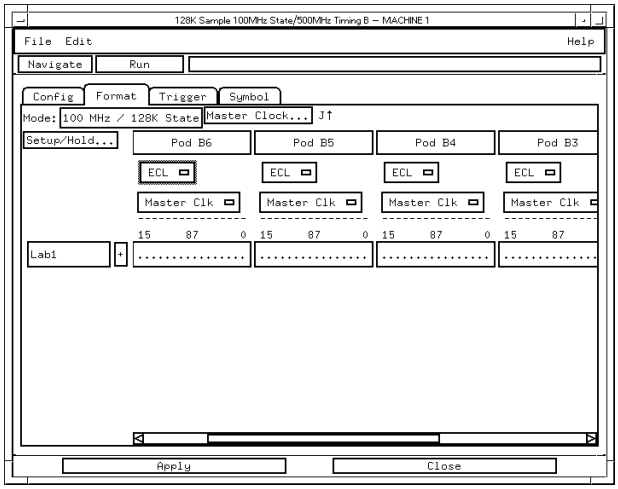
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format tab.

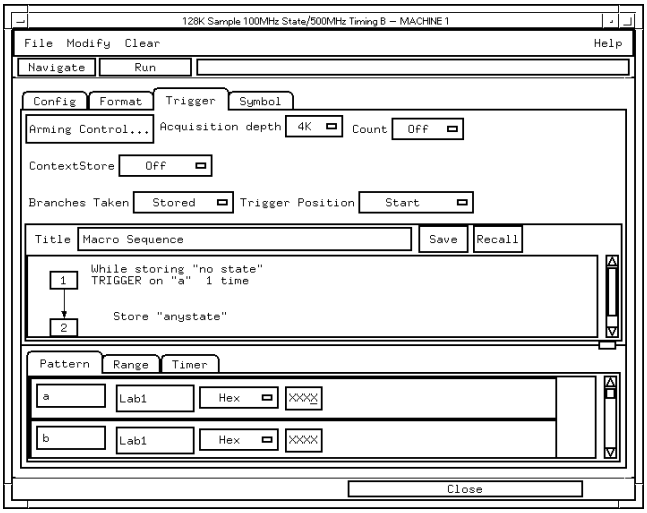
a In the MACHINE 1 setup window, select the Format tab.

b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



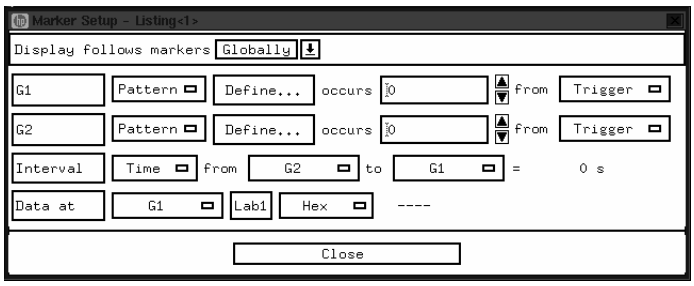
4 Set up the Trigger tab.

- **a** In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.
- **b** Select the Acquisition Depth field, then select “4K”.
- **c** Select the Count field, then select “Off”.
- **d** Select the Trigger Position field, then select Start.
- **e** Click and hold the field labeled “1” in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.



5 Set up the Listing window.

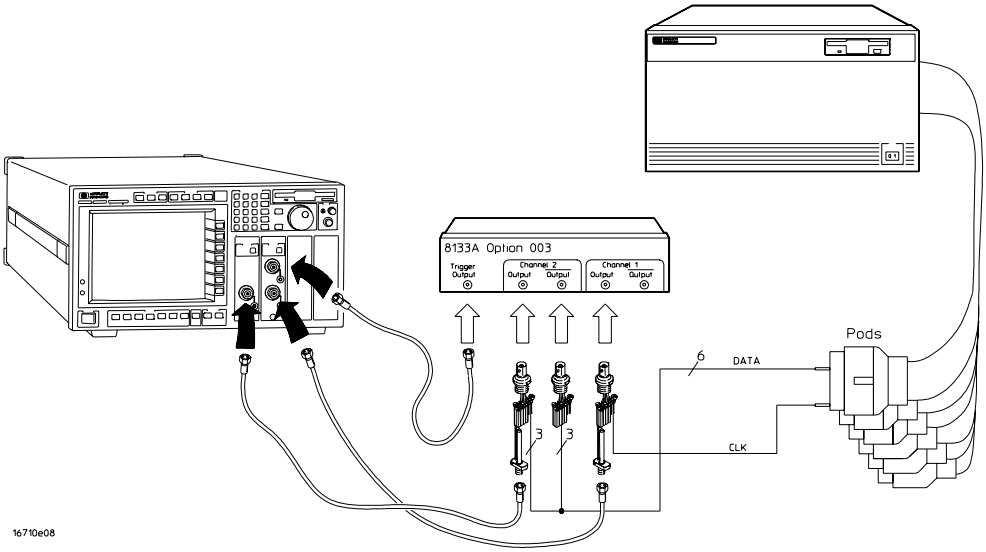
- **a** In the Listing window, select the Markers tab.
- **b** Select the G1: field and the Markers Setup window appears.
- **c** Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.



Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1. Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels.
2. Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table for your logic analysis system.



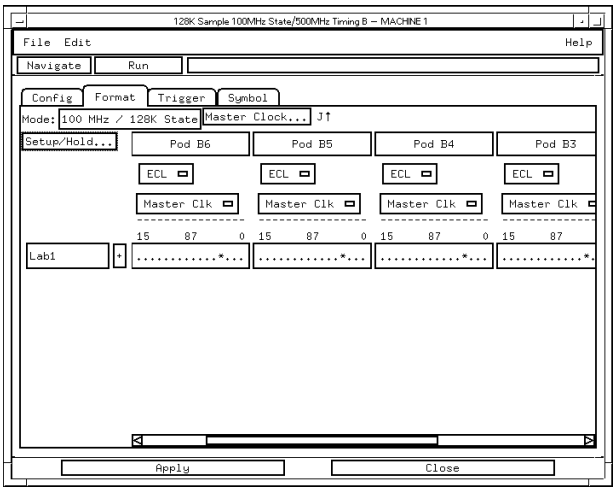
Connect the HP 16710/11/12 to the Pulse Generator

HP 8133A Ch2 Output	HP 8133A Ch2 $\overline{\text{Output}}$	HP 8133A Ch1 Output
First time through this procedure		
Pod 1 channel 3	Pod 2 channel 3	J-clock
Pod 3 channel 3	Pod 4 channel 3	
Pod 5 channel 3	Pod 6 channel 3	
Second time through this procedure		
Pod 1 channel 11	Pod 2 channel 11	J-clock
Pod 3 channel 11	Pod 4 channel 11	
Pod 5 channel 11	Pod 6 channel 11	

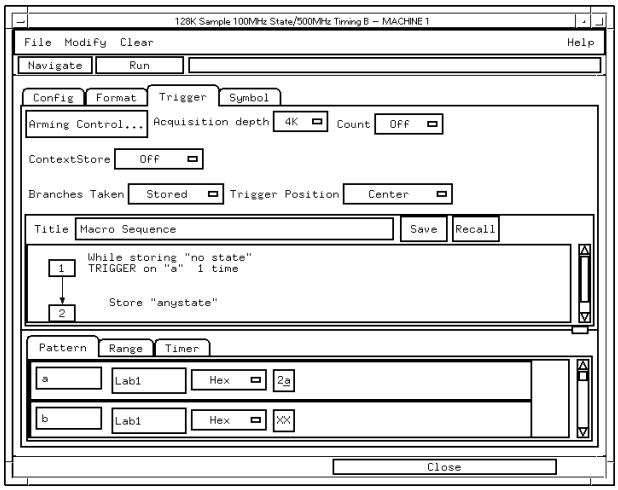
3 Activate the data channels that are connected according to the previous table.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



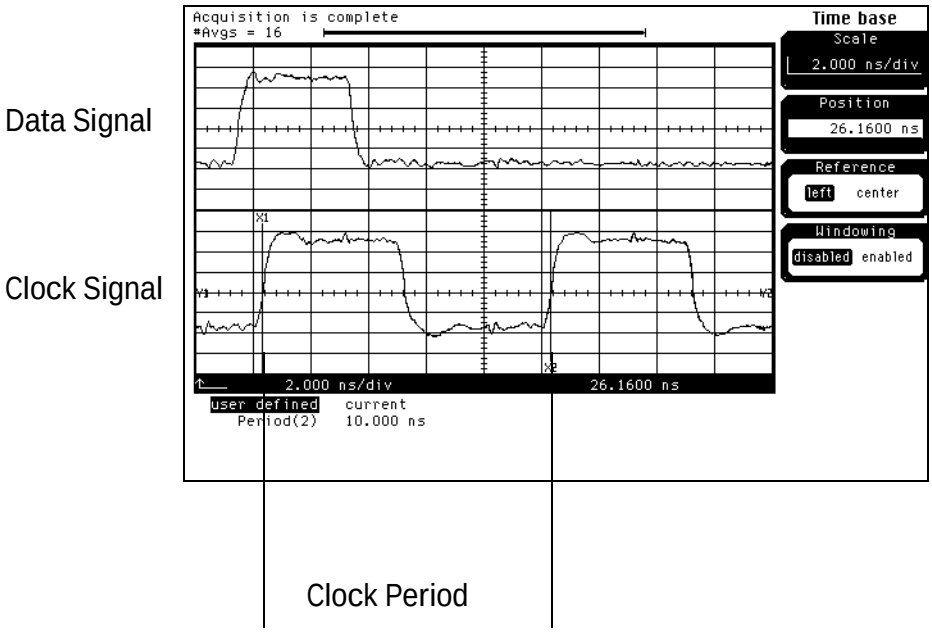
c Under the Trigger tab, select the pattern field associated with pattern recognizer “a”. Enter “2a”.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** Turn on the pulse generator channel 1, channel 2, and trigger outputs.
- **b** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 10.000 ns but greater than 9.750 ns.



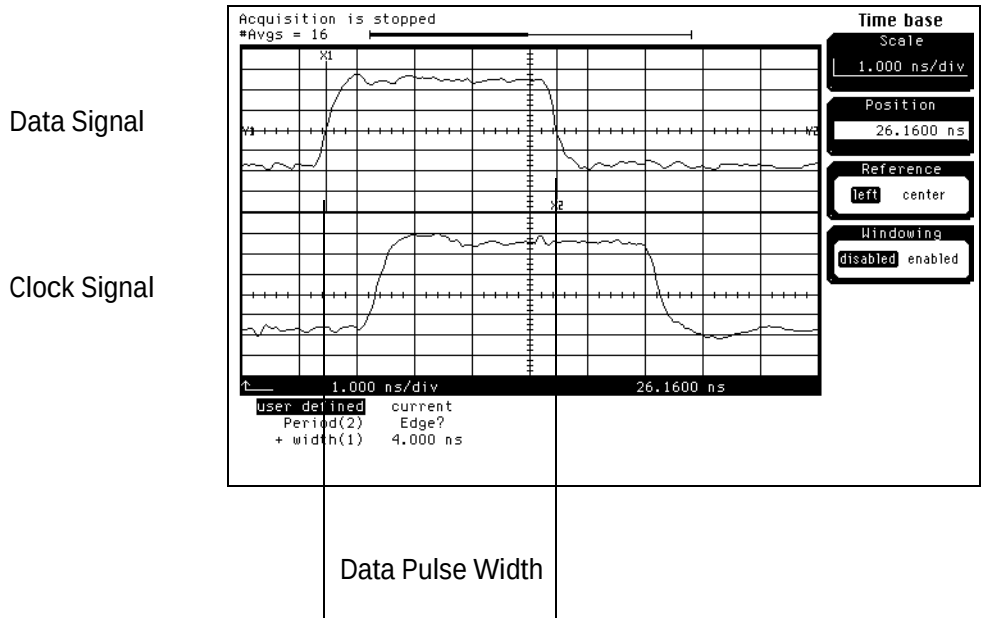
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

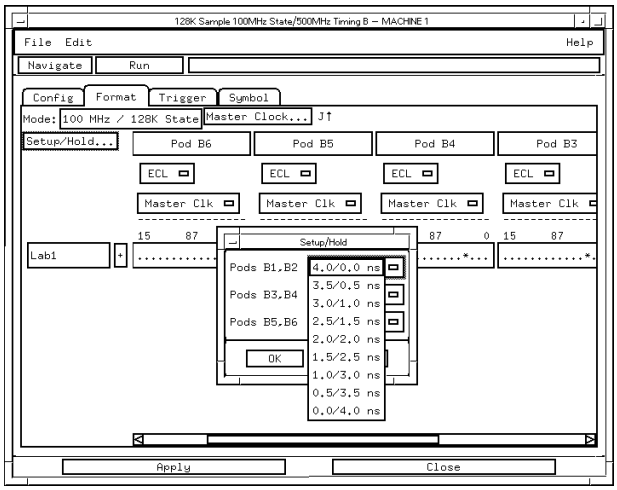
a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select Setup/Hold.

c In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations

4.0/0.0 ns
0.0/4.0 ns



d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

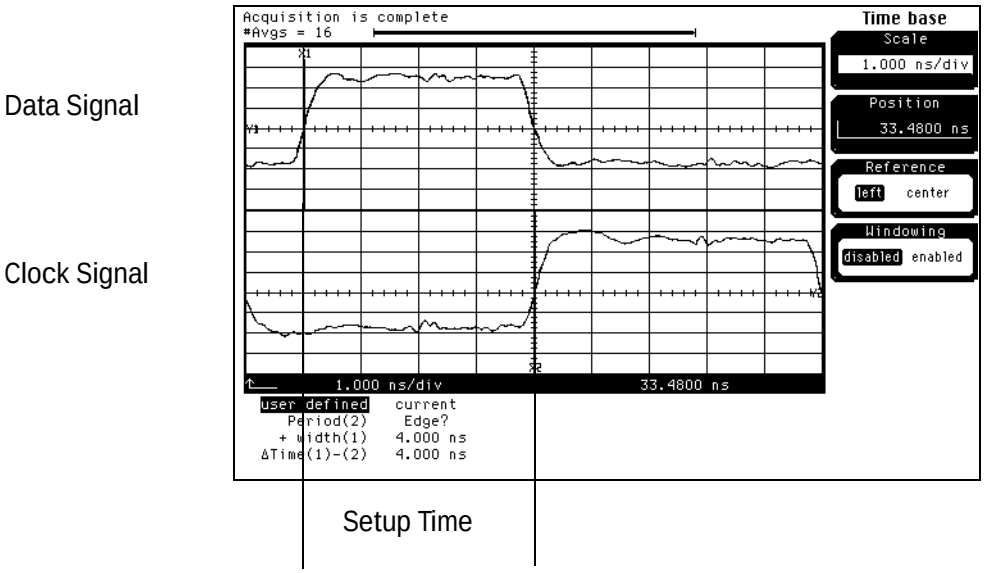
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

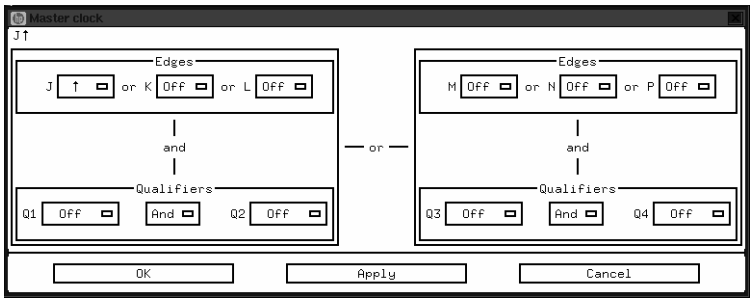
d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



4 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock ...

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Turn off all other clocks. The first time through this test, select the first clock and edge.



Clocks

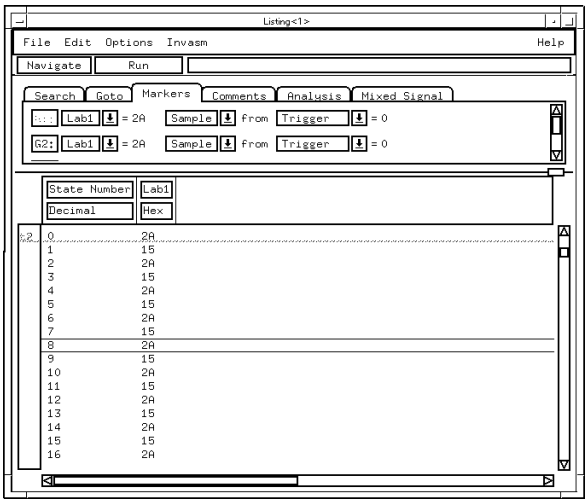
J↑	K↑	L↑	M↑	N↑	P↑

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

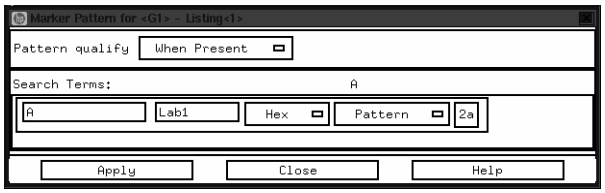
d Select OK to exit the Master Clock menu.

5 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15".



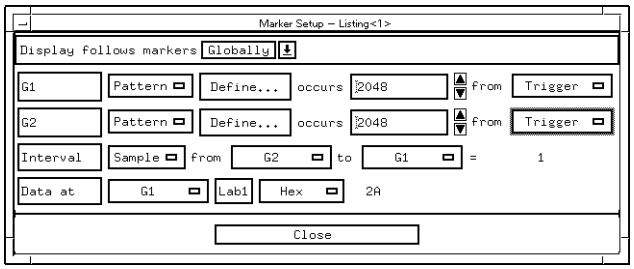
b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “2a”. Select Apply, then select Close.



c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “15”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2048.

e In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the “Pattern NOT found for marker…” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

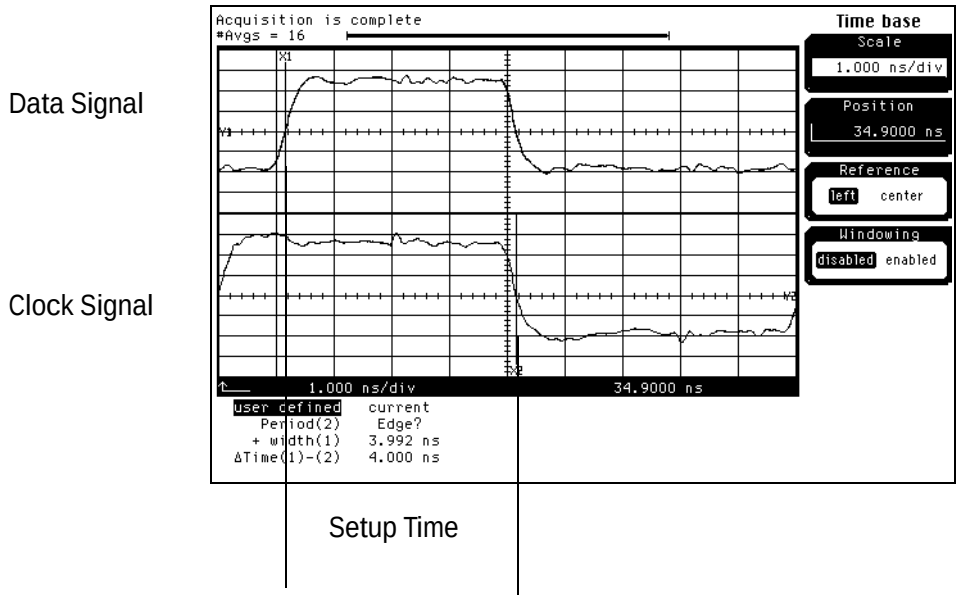
7 Enable the pulse generator channel 1 COMP (LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

b On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

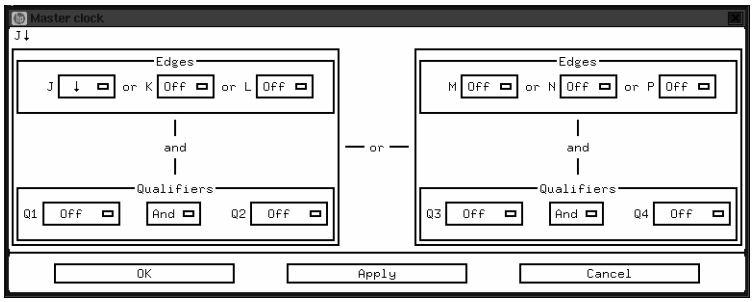
c Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



9 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. The first time through this test, select the first clock and edge. Ensure all other clocks are turned off.



Clocks

J↓	K↓	L↓	M↓	N↓	P↓

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

d Select OK to exit the Master Clock menu.

10 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15".

b If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 9, 10, and 11 for the next clock edge listed in the table in step 9, until all listed clock edges have been tested.

12 If the setup/hold used for the previous steps was 4.0/0.0 ns, repeat steps 1 through 12 using setup/hold 0.0/4.0 ns. If the setup/hold used for the previous steps was 0.0/4.0 ns, continue on with the next section.

Test the next channels

Connect the next combination of data channels and clock channels, and test them. Starting with "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To Test the Multiple-clock, Multiple-edge, State Acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using multiple clocks at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler (Qty 3)	BNC (m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

1 If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer" on page 3-7. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

2 Change the pulse generator channel 2 width to 5.000 ns.

Set up the logic analyzer

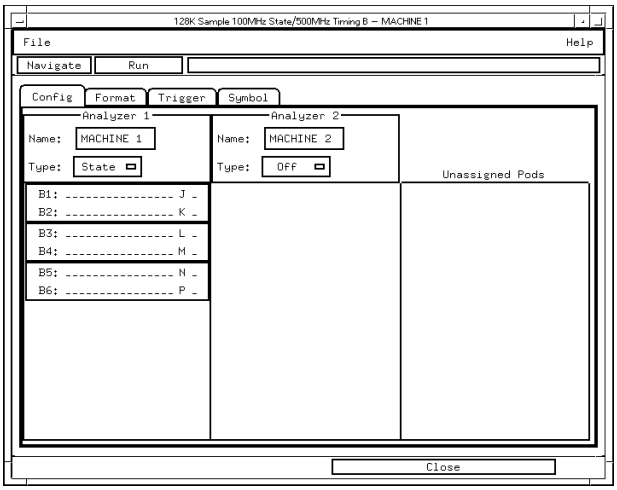
Perform the following steps if you have not already done so for the previous test.

1 Set up the Configuration tab.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 box, select Timing, then in the pop-up menu select State.

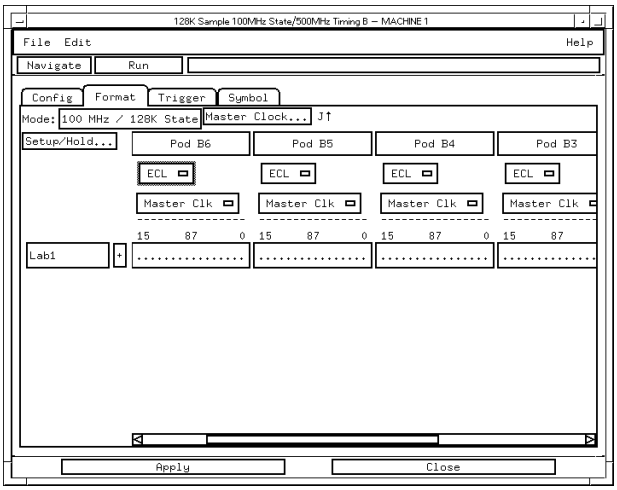
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format tab.

a In the MACHINE 1 setup window, select the Format tab.

b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



4 Set up the Trigger tab.

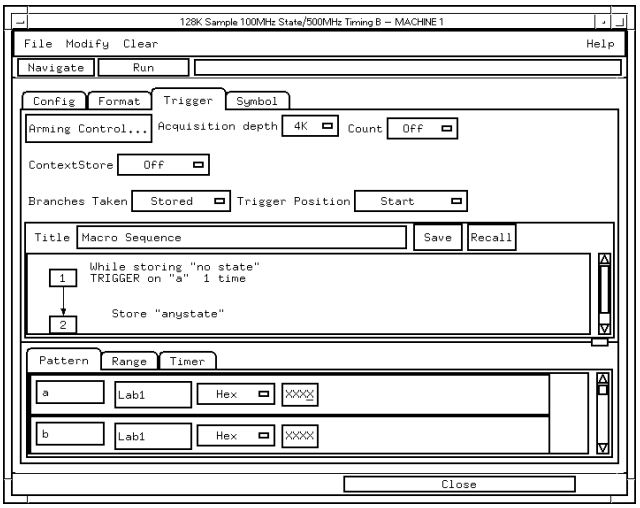
a In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Click and hold the field labeled “1” in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.

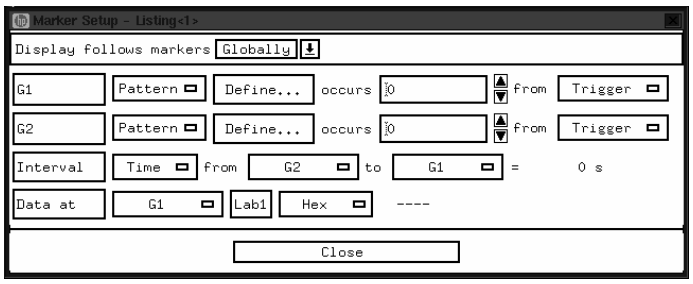


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

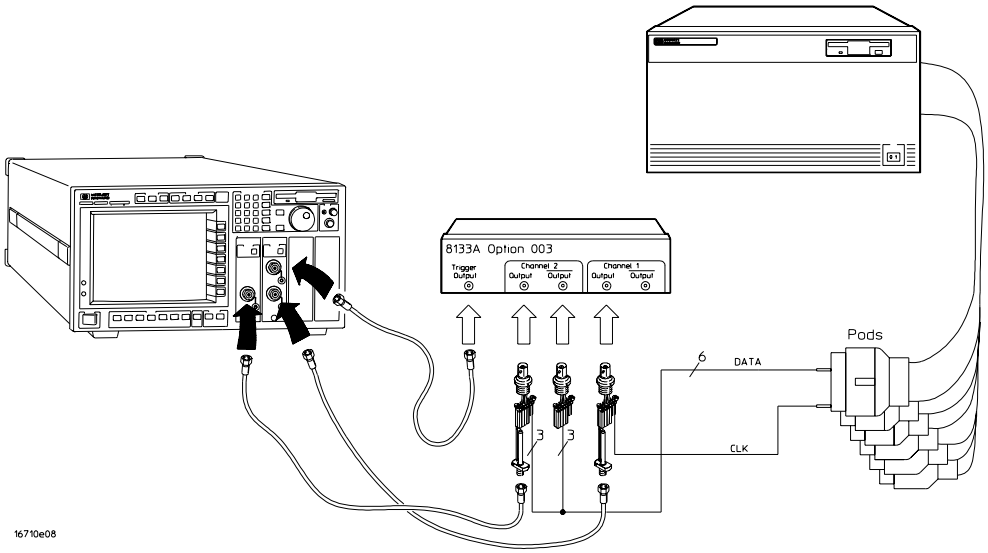


Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following table to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table.



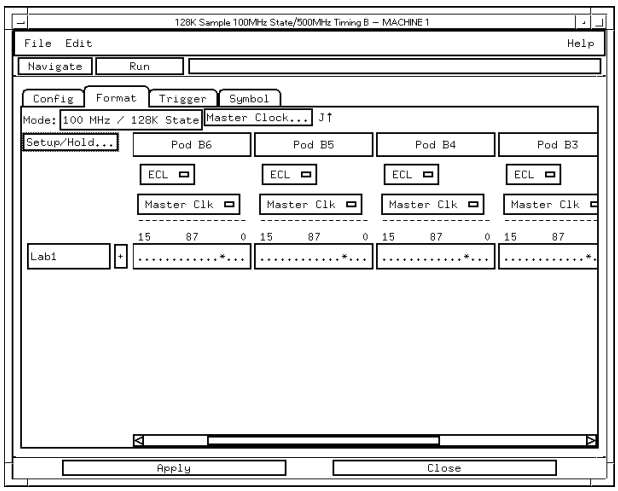
Connect the HP 16710/11/12 to the Pulse Generator

HP 8133A Ch2 Output	HP 8133A Ch2 $\overline{\text{Output}}$	HP 8133A Ch1 Output
First time through this procedure		
Pod 1 channel 3	Pod 2 channel 3	J-clock
Pod 3 channel 3	Pod 4 channel 3	L-clock
Pod 5 channel 3	Pod 6 channel 3	N-clock
Second time through this procedure		
Pod 1 channel 11	Pod 2 channel 11	J-clock
Pod 3 channel 11	Pod 4 channel 11	L-clock
Pod 5 channel 11	Pod 6 channel 11	N-clock

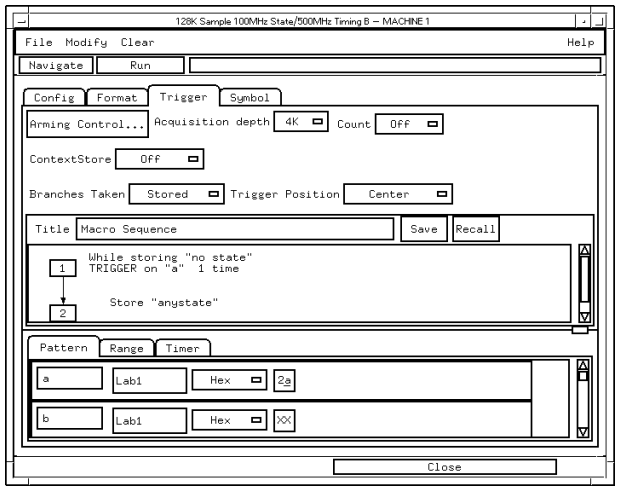
3 Activate the data channels that are connected according to the previous table.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



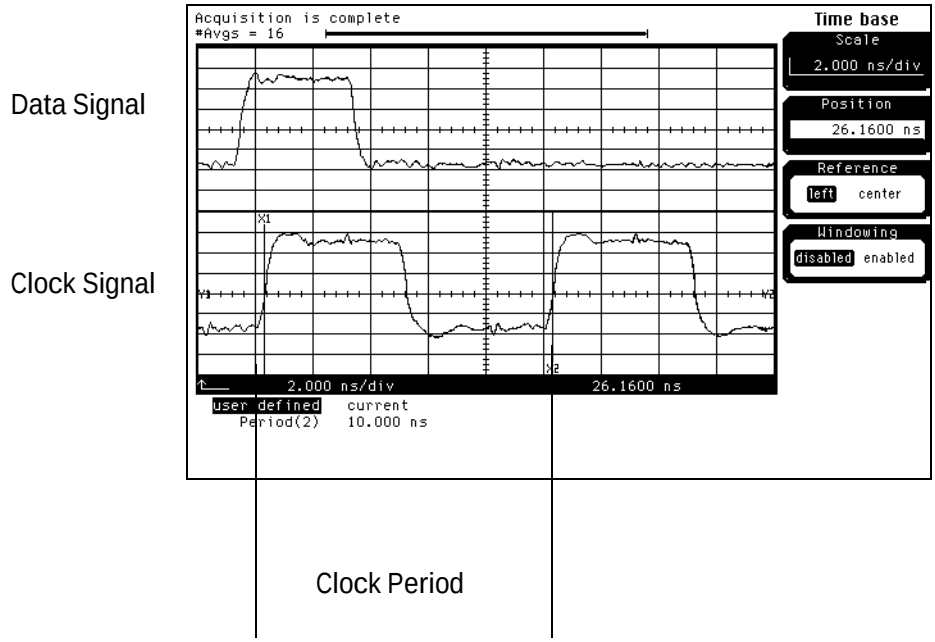
c Under the Trigger tab, select the pattern field associated with pattern recognizer “a”. Enter “2a”.



Verify the test signal

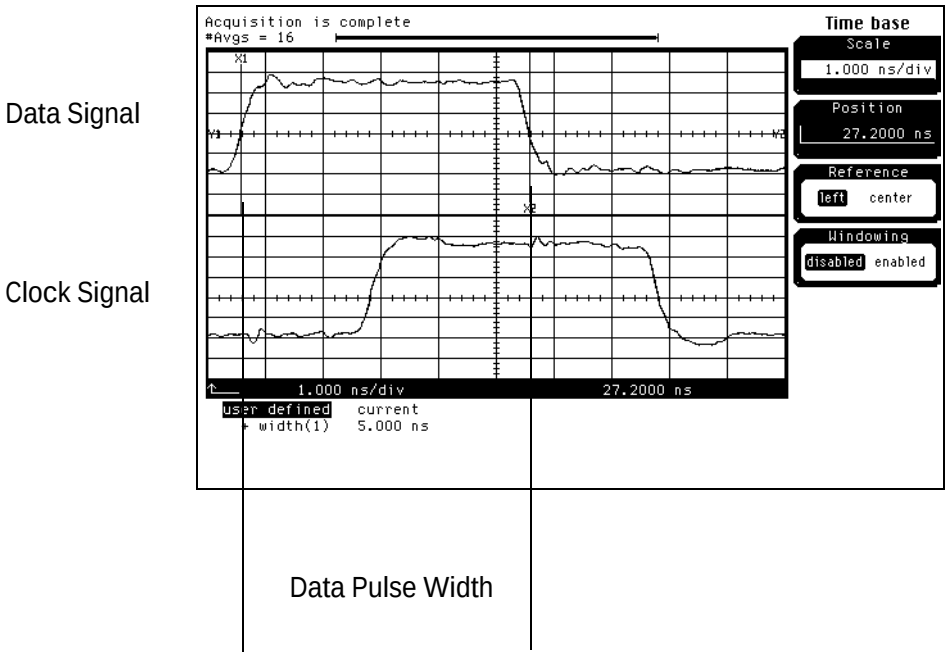
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or - 250 ps.

- **a** Turn on the pulse generator channel 1, channel 2, and trigger outputs.
- **b** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 10.000 ns but greater than 9.750 ns.



2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 5.000 ns, +0 ps or - 100 ps.

- **a** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **b** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.
- **c** On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).
- **d** If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select Master Clock… Select and activate any two clock edges, then select OK.

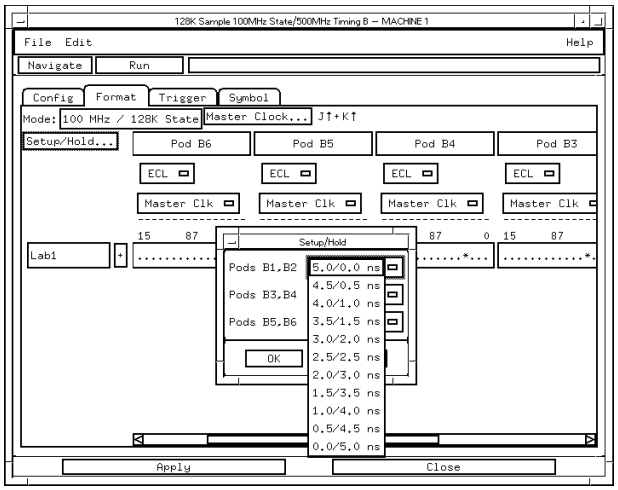
The Setup/Hold window requires two single-edge clocks before it will allow a setup/hold of 5.0/0.0 ns.

c Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations

5.0/0.0 ns
0.0/5.0 ns



e Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

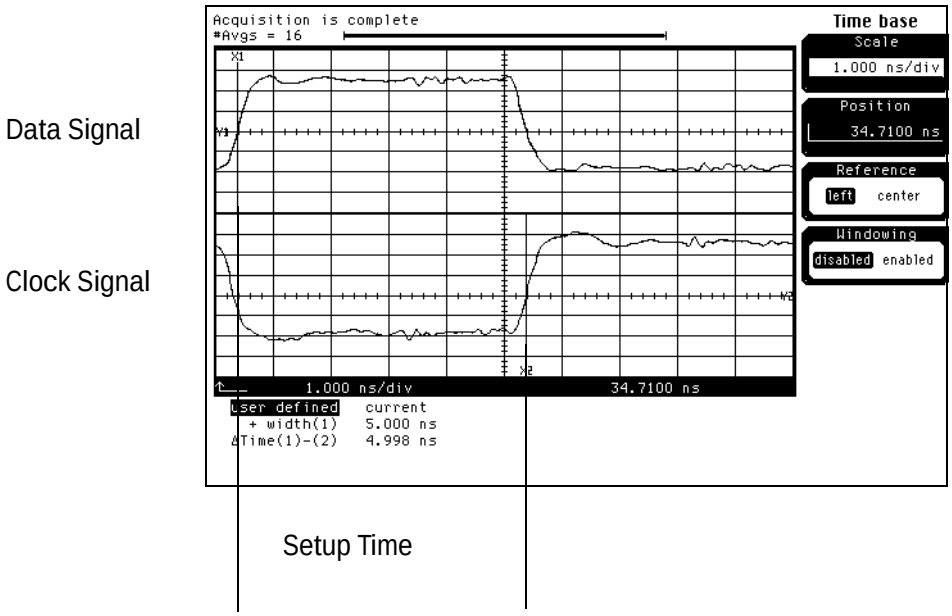
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

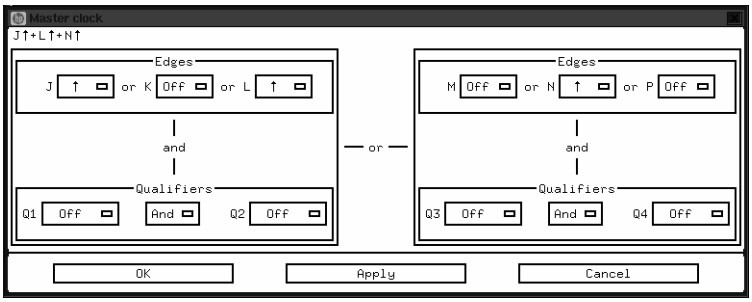
d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



4 Select the clock combination to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Turn off all other clocks. The first time through this test, select the first clock combination.



Clock Combinations

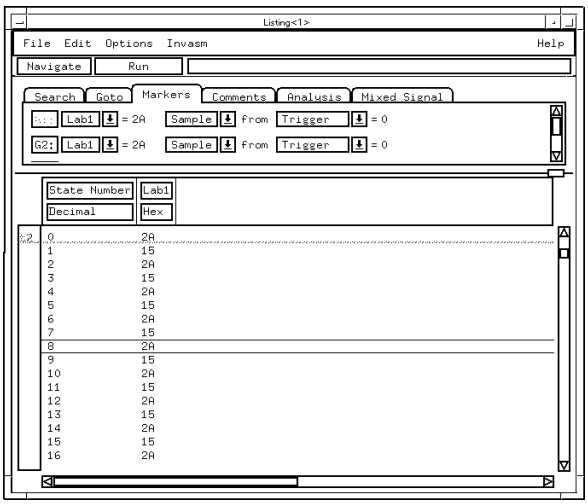
J↑ + L↑ + N↑	K↑ + M↑ + P↑

c Select OK.

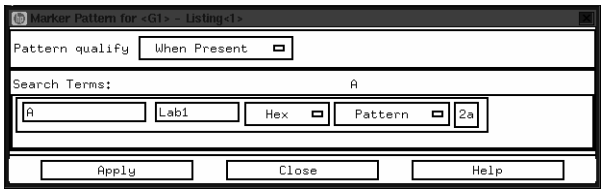
d Connect the clock input channels to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

5 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15".



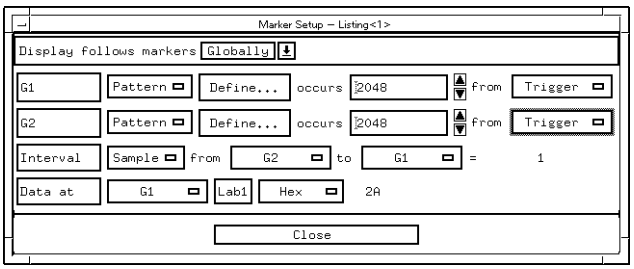
b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “2a”. Select Apply, then select Close.



c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “15”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2048.

e In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the “Pattern NOT found for marker...” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Test the next clock combination.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 4, 5, and 6 for the next clock edge combination listed in the table in step 4, until both clock combinations have been tested.

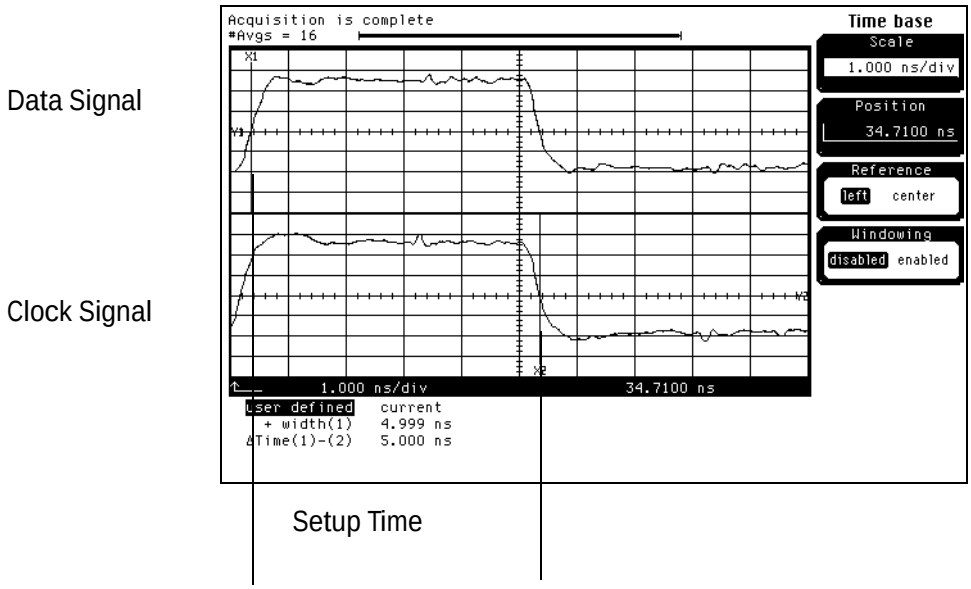
7 Enable the pulse generator channel 1 COMP (LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

b On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



9 Select the clock combination to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b In the Master Clock window, select the edge field next to the clocks to be tested, then select the clock edges as indicated in the table. Turn off all other clocks. The first time through this test, select the first clock combination.

Clock Combinations

J↓ + L↓ + N↓	K↓ + M↓ + P↓

c Connect the clock input channels to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

d Select OK to exit the Master Clock menu.

10 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15".

b If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 Test the next clock combination.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 9, 10, and 11 for the next clock combination listed in the table in step 9, until both clock combinations have been tested.

12 If the setup/hold used for the previous steps was 5.0/0.0 ns, repeat steps 1 through 12 using setup/hold 0.0/5.0 ns. If the setup/hold used for the previous steps was 0.0/5.0 ns, continue on with the next section.

Test the next channels

Connect the next combination of data channels and clock channels, and test them. Starting with "Connect the logic analyzer" on page 3-32 connect the next combination, then continue through the complete test.

To Test the Single-clock, Multiple-edge, State Acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using a multiple-edge single clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler (Qty 3)	BNC (m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

1 If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer" on page 3-7. Use the pulse generator settings listed below.

2 Make the following changes to the pulse generator configuration.

Timebase	Channel2
Period: 20.000 ns	Divide: PULSE ÷ 1 Width: 4.500 ns

Set up the logic analyzer

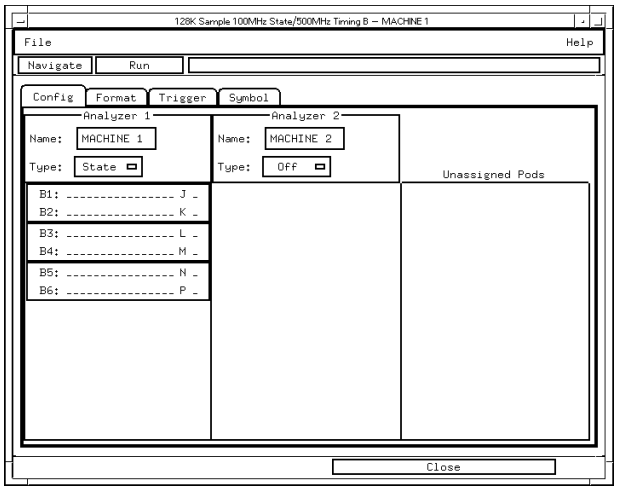
Perform the following steps if you have not done so for the previous tests.

1 Set up the Configuration tab.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 Type box select Timing, then in the pop-up menu select State.

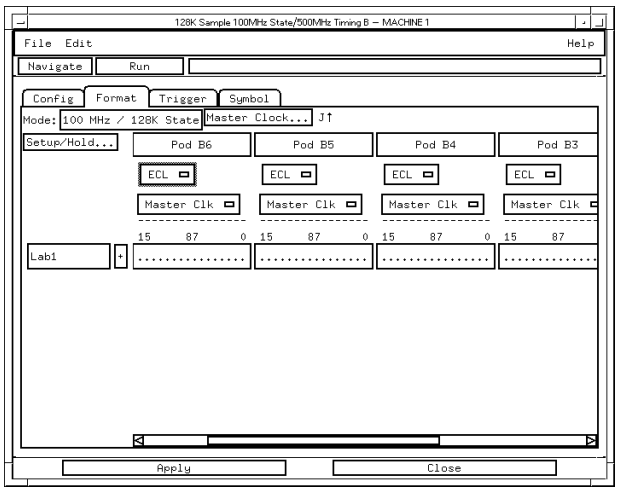
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format tab.

a In the MACHINE 1 setup window, select the Format tab.

b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



4 Set up the Trigger tab.

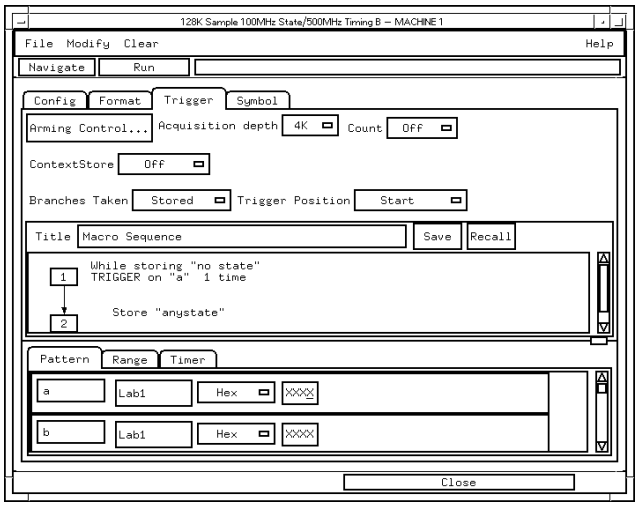
a In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Click and hold the field labeled “1” in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.

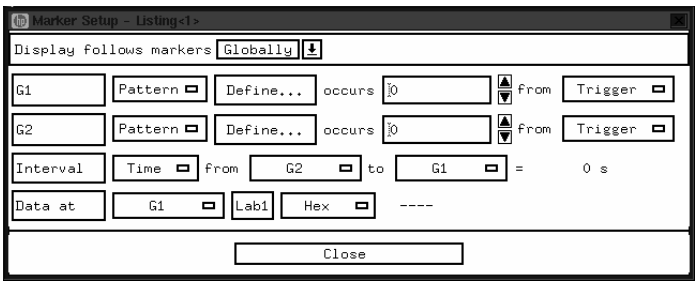


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

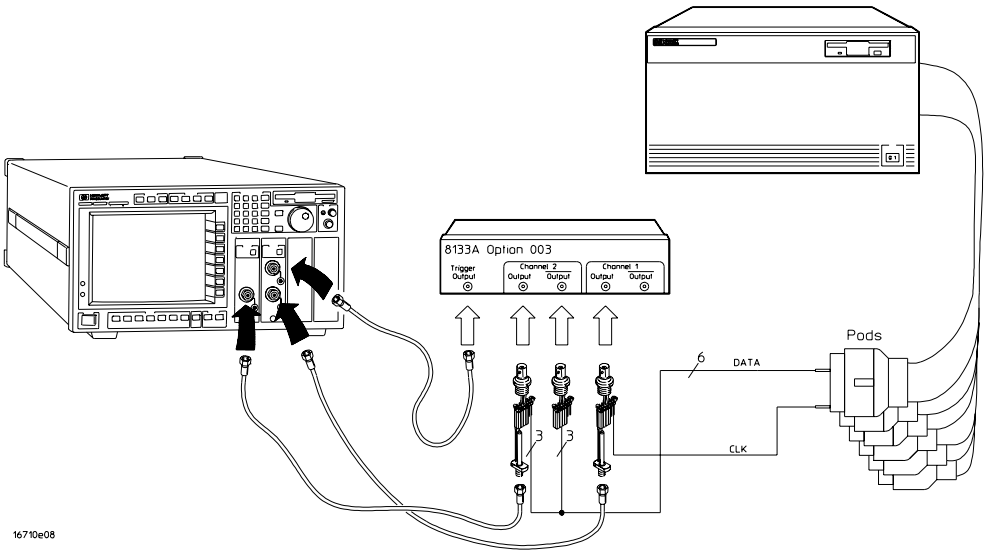
c Select the Sample field associated with G1, and select Pattern. Select the Sample field associated with G2, and select Pattern.



Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1. Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels.
2. Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table.



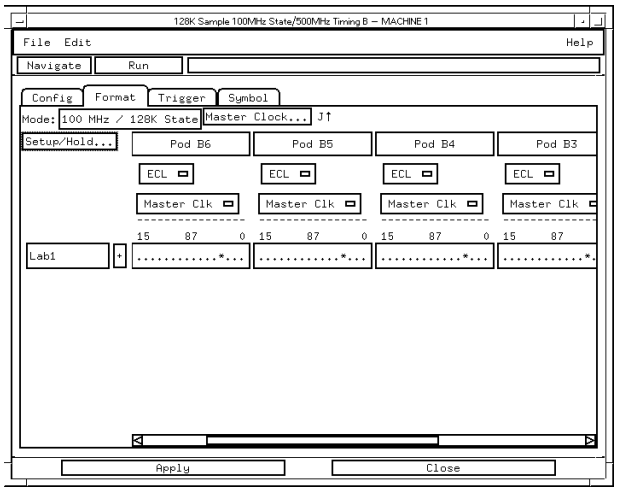
Connect the HP 16710/11/12 to the Pulse Generator

HP 8133A Ch2 Output	HP 8133A Ch2 $\overline{\text{Output}}$	HP 8133A Ch1 Output
First time through this procedure		
Pod 1 channel 3	Pod 2 channel 3	J-clock
Pod 3 channel 3	Pod 4 channel 3	
Pod 5 channel 3	Pod 6 channel 3	
Second time through this procedure		
Pod 1 channel 11	Pod 2 channel 11	J-clock
Pod 3 channel 11	Pod 4 channel 11	
Pod 5 channel 11	Pod 6 channel 11	

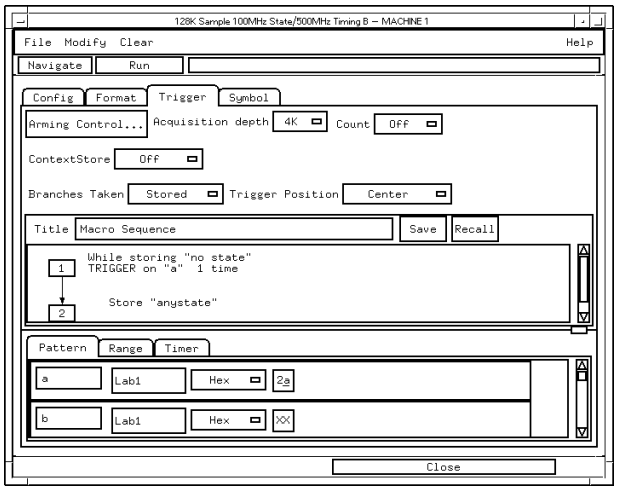
3 Activate the data channels that are connected according to the previous table.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



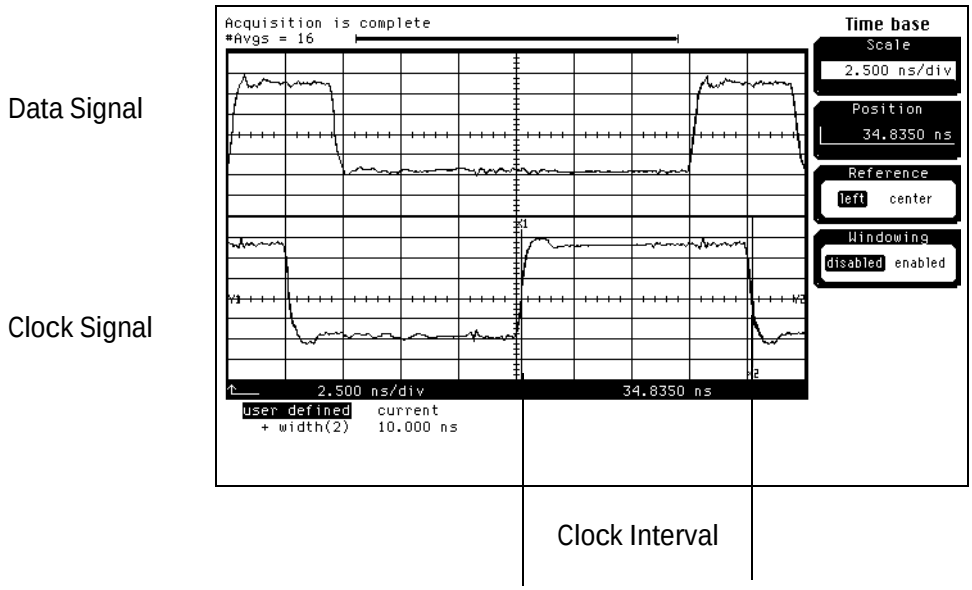
c Under the Trigger tab, select the pattern field associated with pattern recognizer “a”. Enter “2a”.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** Turn on the pulse generator channel 1, channel 2, and trigger outputs.
- **b** In the oscilloscope Timebase menu, select Scale: 2.500 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 10.000 ns, go to step e. If the positive-going pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **f** Decrease the pulse generator Period in 10 ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 10.000 ns, but greater than 9.750 ns.



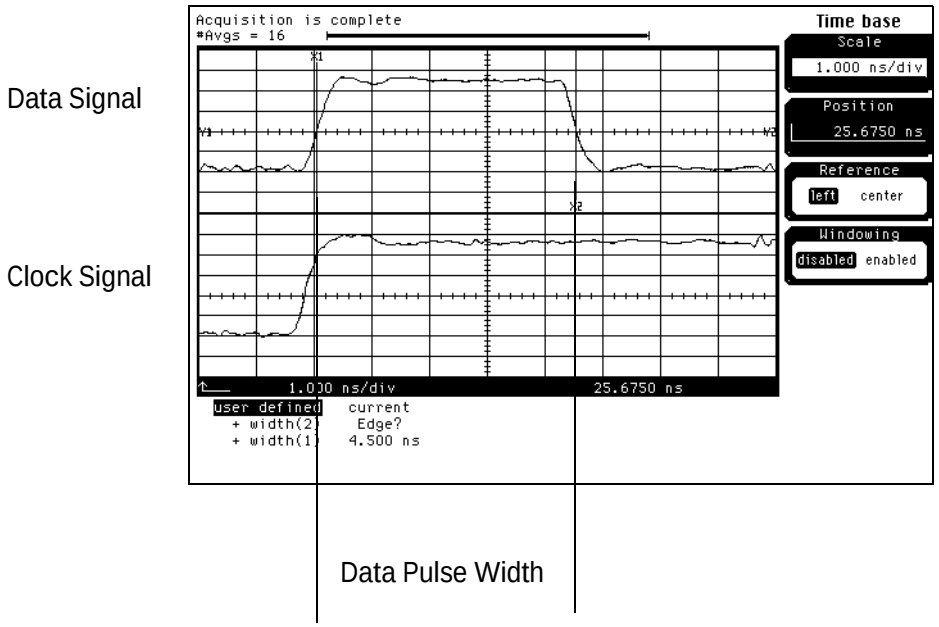
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.500 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b In the Master Clock window, activate a rising and falling edge (↕) for any clock, then select OK.

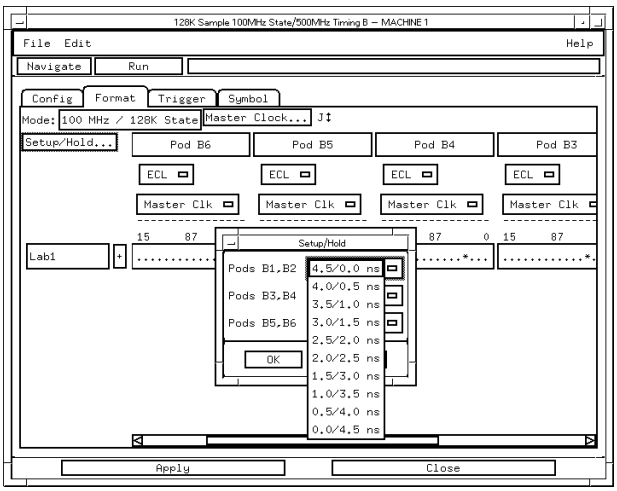
The Setup/Hold window requires a double clock edge before it will allow a setup/hold of 4.5/0.0 ns.

c Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations

4.5/0.0 ns
0.0/4.5 ns



e Select OK to exit the Setup/Hold window.

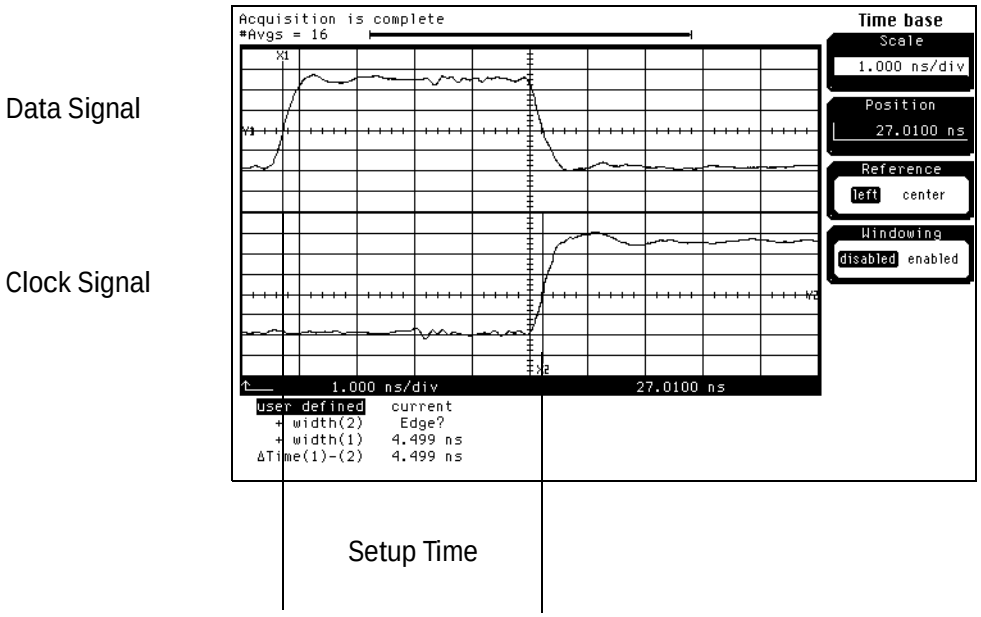
2 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

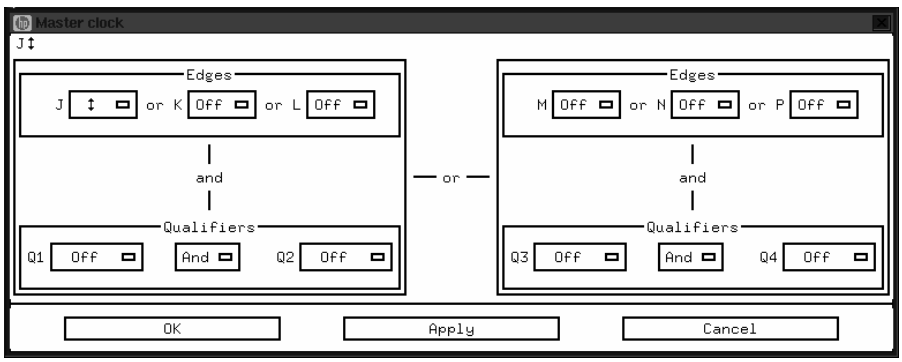
d Adjust the pulse generator channel 2 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



3 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Ensure all other clocks are turned off. The first time through this test, select the first clock and edge.



Clocks

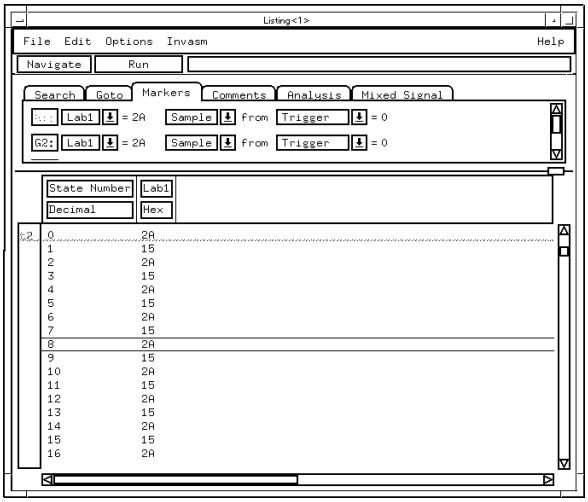
J↕	K↕	L↕	M↕	N↕	P↕

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

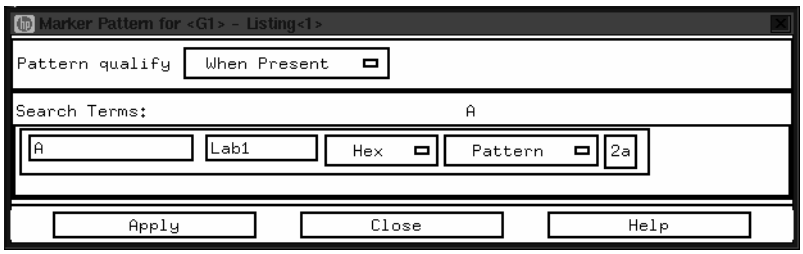
d Select OK to exit the Master Clock menu.

4 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15".



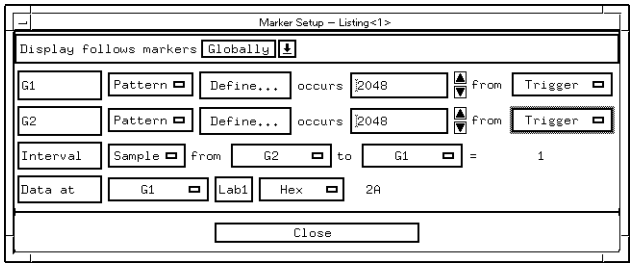
b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter "2a". Select Apply, then select Close.



c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter "15". Select Apply, then select Close.

d In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 2048.

e In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

5 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 3, 4, and 5 for the next clock edge listed in the table in step 3, until all listed clock edges have been tested.

6 If the setup/hold used for the previous steps was 4.5/0.0 ns, repeat steps 1 through 5 using setup/hold 0.0/4.5 ns. If the setup/hold used for the previous steps was 0.0/4.5 ns, continue on with the next section.

Test the next channels

Connect the next combination of data channels and clock channels, and test them.

Starting with "Connect the logic analyzer" on page 3-45, connect the next combination, then continue through the complete test.

To Test the Time Interval Accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125-MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 Mhz, 3.5 ns pulse width, < 600 ps rise time	HP 8133A Option 003
Function Generator	Accuracy ≤ (5)(10^{-6}) x frequency	HP 8656B Option 002
SMA Coax Cable	18 GHz Bandwidth	HP 8120-4948
BNC Cable		HP 8120-1840
Adapter	SMA(m)-BNC(f)	HP 1250-1200
Adapter	BNC(m)-SMA(f)	HP1250-2015
Coupler	BNC(m-m)	HP 1250-0216
BNC Test Connector, 6x2		

Set up the equipment

1 If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer" on page 3-7.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

3 Set up the function generator according to the following table.

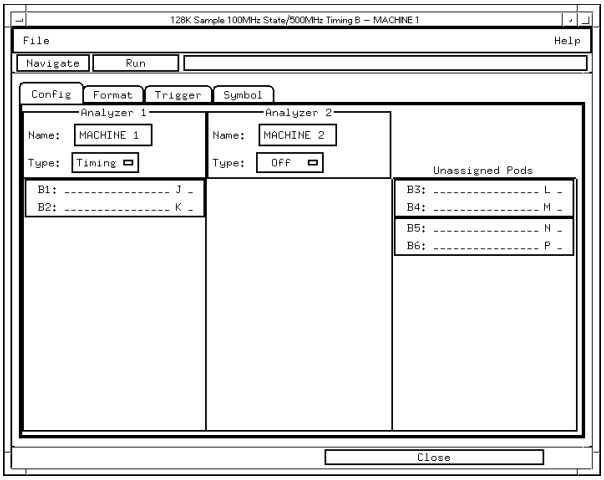
Function Generator Setup

Freq: 40.000 00 MHz	Amptd: 1.00 V	Modulation: Off

Set up the logic analyzer

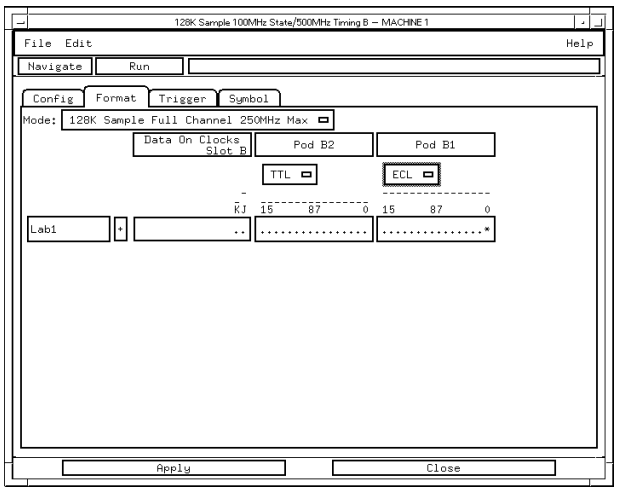
1 Set up the Config tab.

- **a** In the MACHINE 1 window, select the Config tab.
- **b** In the Analyzer 1 box, select State, then in the pop-up menu select Timing.
- **c** Unassign all pods from Analyzer 1 except for Pod 1 and 2. To deassign the remaining pods, drag and drop the pods to the Unassigned Pods column using the mouse. Only Pods 1 and 2 should remain assigned to Analyzer 1.



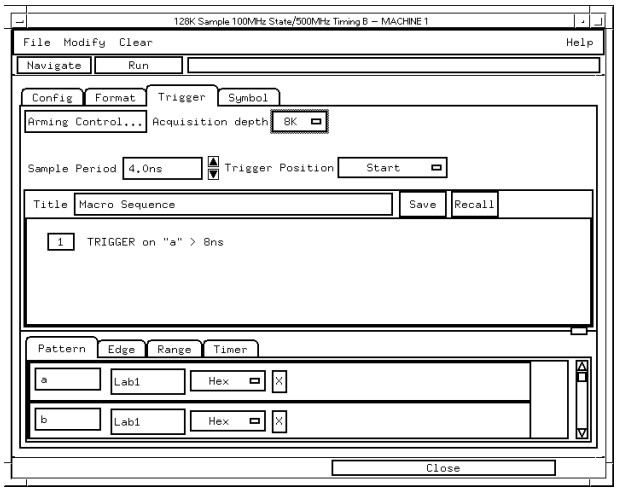
2 Set up the Format tab.

- **a** In the MACHINE 1 setup window, select the Format tab.
- **b** Under the Pod 1 field, select TTL, then select ECL.
- **c** Under the Format tab, select the field showing the channel assignments for Pod 1. Using the mouse, first clear the channels (all "."), then select channel 0. An asterisk means that the channel is turned on.



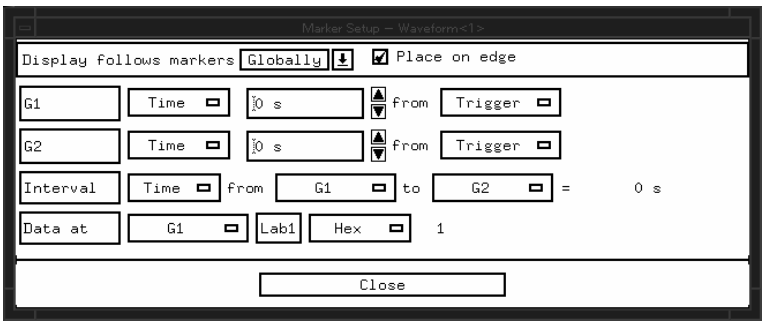
3 Set up the Trigger tab.

- **a** In the MACHINE 1 setup window, select the Trigger tab. Select Clear, then select All.
- **b** Select the Acquisition Depth field, then select “8K”.
- **c** Under the Trigger tab, select Trigger Position, then select Start.
- **d** Select the sample period value field, then enter 4.0.



4 Set up the Waveform window.

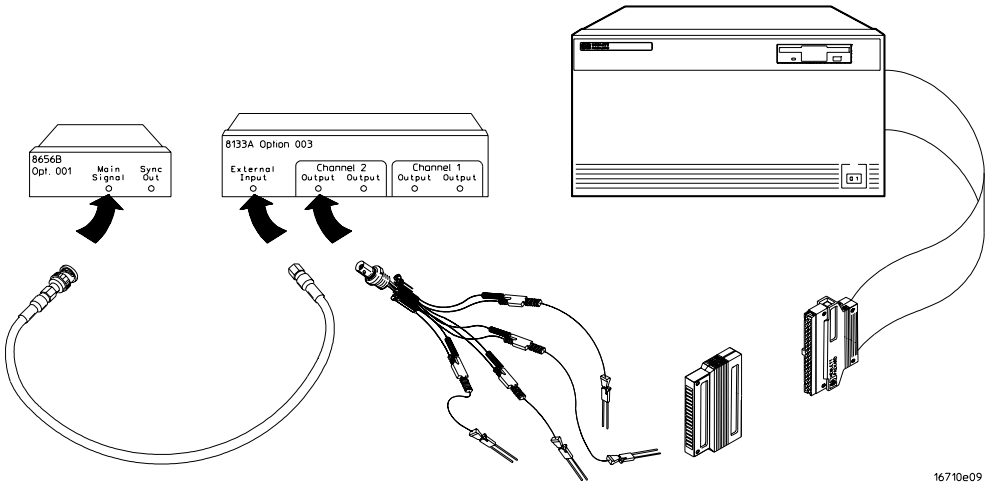
- **a** In the MACHINE 1 window, select Navigate, then select Slot n: MACHINE 1 (where “n” is the slot you have the module installed), then select Waveform. A Waveform window will now open.
- **b** In the Waveform window select the Markers tab.
- **c** Select the G1 field and a Marker Setup window appears.
- **d** Ensure that the Interval Time field reads “from G1 to G2” (instead of “from G2 to G1”).



Leave this window open as you will be using it later when acquiring data.

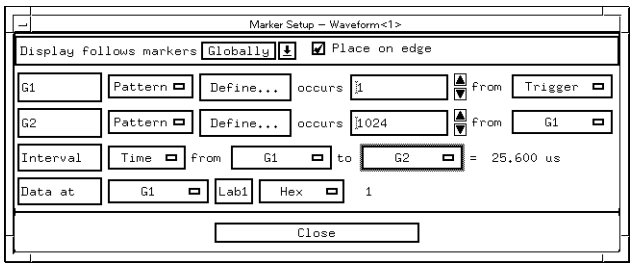
Connect the logic analyzer

1. Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 2 output.
2. Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



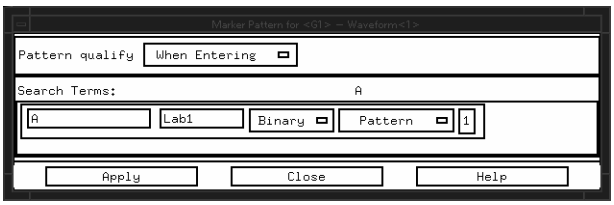
Acquire the data

1. Enable the pulse generator channel 2 and trigger outputs (with the LED off).
2. In the logic analyzer Waveform window, select Run.
3. Configure the markers to measure the time interval.
   - **a** In the Marker Setup window select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select pattern.
   - **b** Select the Occurs field associated with G1 and enter “1”. Select the Occurs field associated with G2 and enter “1024”.
   - **c** Select the From field associated with G2 and select G1.



In the Marker Setup Window, you will observe the Interval Time from G1 to G2=value to determine the pass or fail status of this test.

d In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the Pattern field, enter “1”. Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.



e In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the Pattern field, enter “1”. Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.

4 Acquire the data.

a In the Waveform window, move the mouse cursor over Run and click and hold the right mouse button. At the pop-up menu, select Repetitive.

b Select Run. The logic analyzer repetitively acquires data.

c Continuously observe the Interval Time from G1 to G2=value in the Marker Setup window.

Allow the logic analyzer to run repetitively for approximately one minute. If the Interval Time value remains inside the range 25.592 µs to 25.608 µs, the test passes. Record a Pass or Fail in the performance test record.

d Select Stop to end the acquisition.

To Test the Two-card Module

The two-card test is only required for configured two-card modules. Performing the test verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

Two-card modules that were changed to one-card modules for the previous performance tests need to be reconfigured as two-card modules for this test.

This test checks a combination of data channels using a single-edge clock at one selected setup/hold time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	100 Mhz, 3.5 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A w/ HP 54751A
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler (Qty 3)	BNC (m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 3-7. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

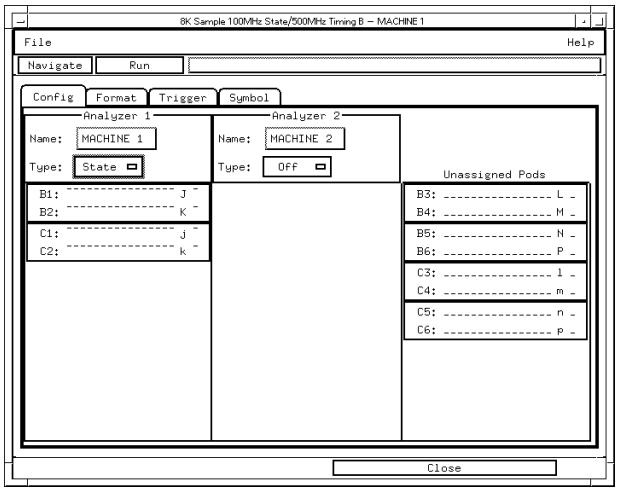
Set up the logic analyzer

1 Set up the Configuration tab.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 Type box select Timing, then in the pop-up menu select State.

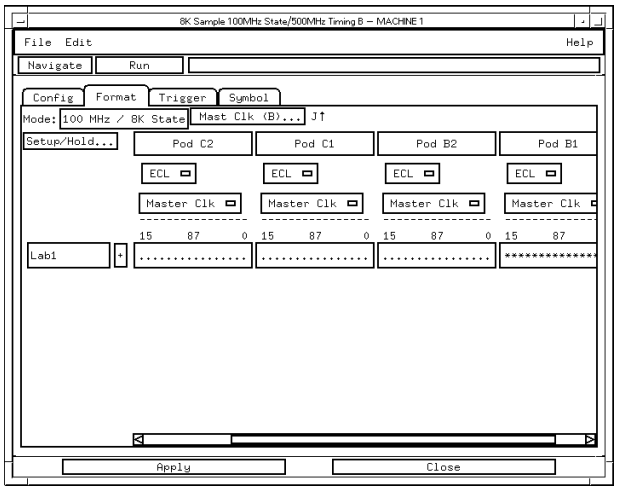
2 Under the Config tab, assign pods 1 and 2 of both the master and expander cards to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format tab.

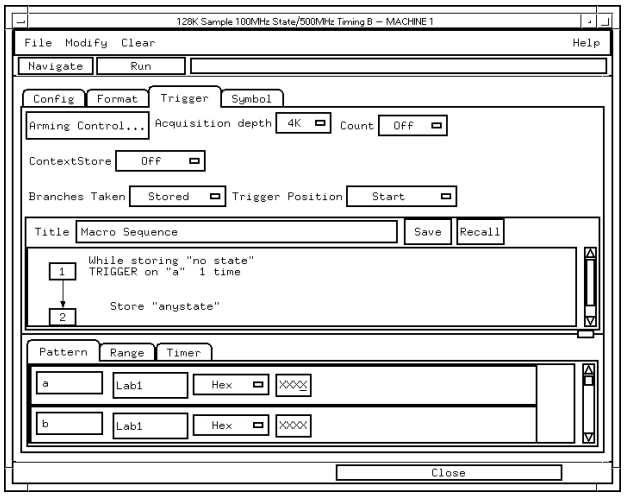
a In the MACHINE 1 setup window, select the Format tab.

b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



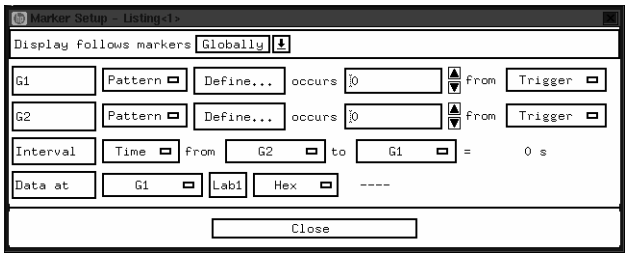
4 Set up the Trigger tab.

- **a** In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.
- **b** Select the Acquisition Depth field, then select “4K”.
- **c** Select the Count field, then select “Off”.
- **d** Select the Trigger Position field, then select Start.
- **e** Click and hold the field labeled “1” in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.



5 Set up the Listing window.

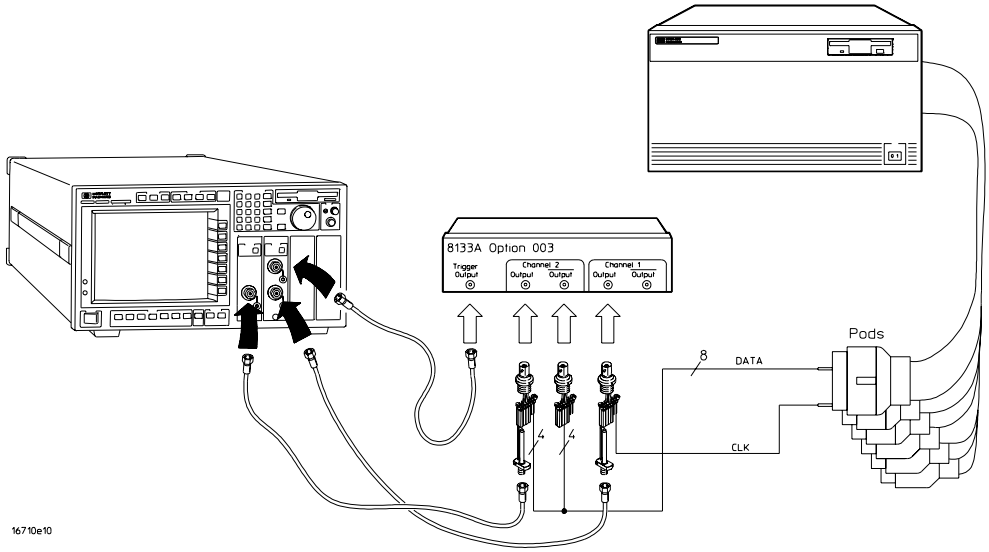
- **a** In the Listing window, select the Markers tab.
- **b** Select the G1: field and the Markers Setup window appears.
- **c** Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.



Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1. Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator.
2. Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table for your logic analysis system.



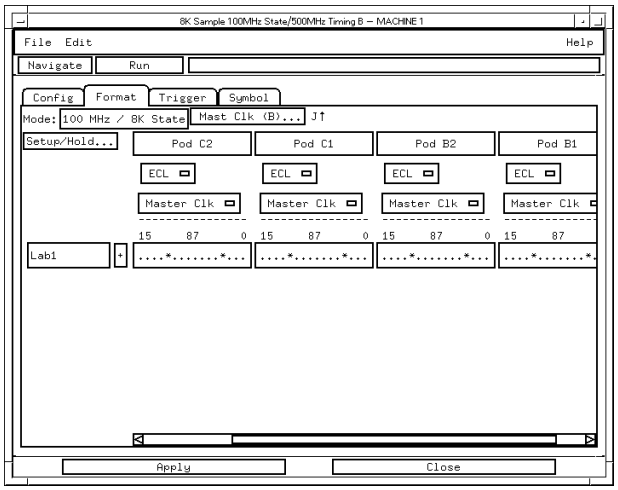
Connect the HP 16710/11/12 to the Pulse Generator

HP 8133A Ch2 Output	HP 8133A Ch2 $\overline{\text{Output}}$	HP 8133A Ch1 Output
Master card		
Pod 1 channel 3	Pod 1 channel 11	J-clock
Pod 2 channel 3	Pod 2 channel 11	
Expander card		
Pod 1 channel 3	Pod 1 channel 11	
Pod 2 channel 3	Pod 2 channel 11	

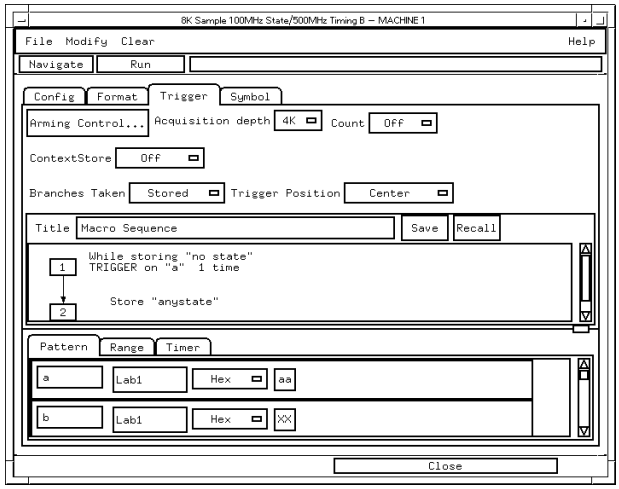
3 Activate the data channels that are connected according to the previous table.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select channels 3 and 11. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



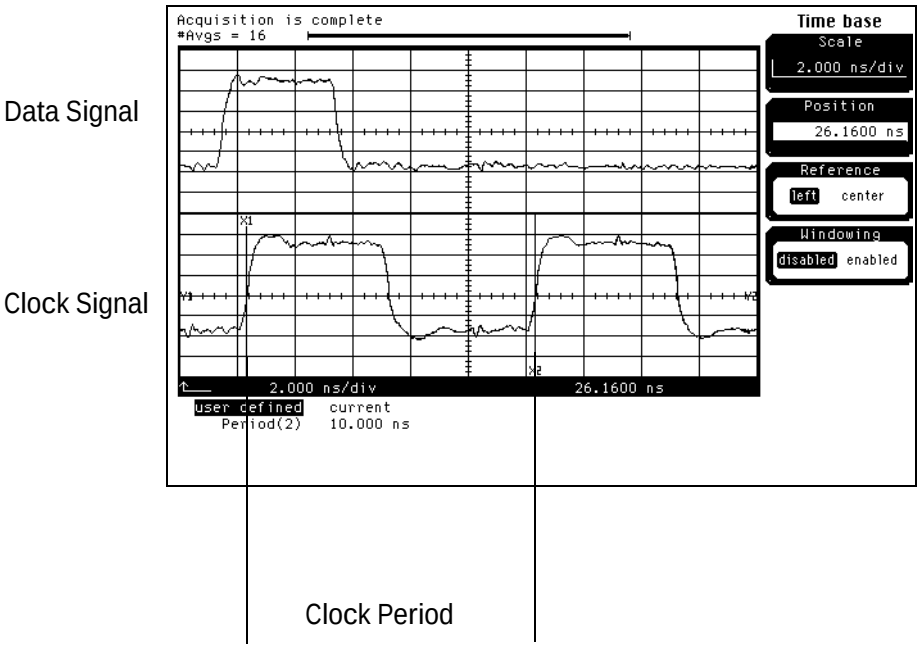
c Under the Trigger tab, select the pattern field associated with pattern recognizer “a”. Enter “aa”.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** Turn on the pulse generator channel 1, channel 2, and trigger outputs.
- **b** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than 10.000 ns but greater than 9.750 ns, go to step 3.
- **e** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 10.000 ns but greater than 9.750 ns.



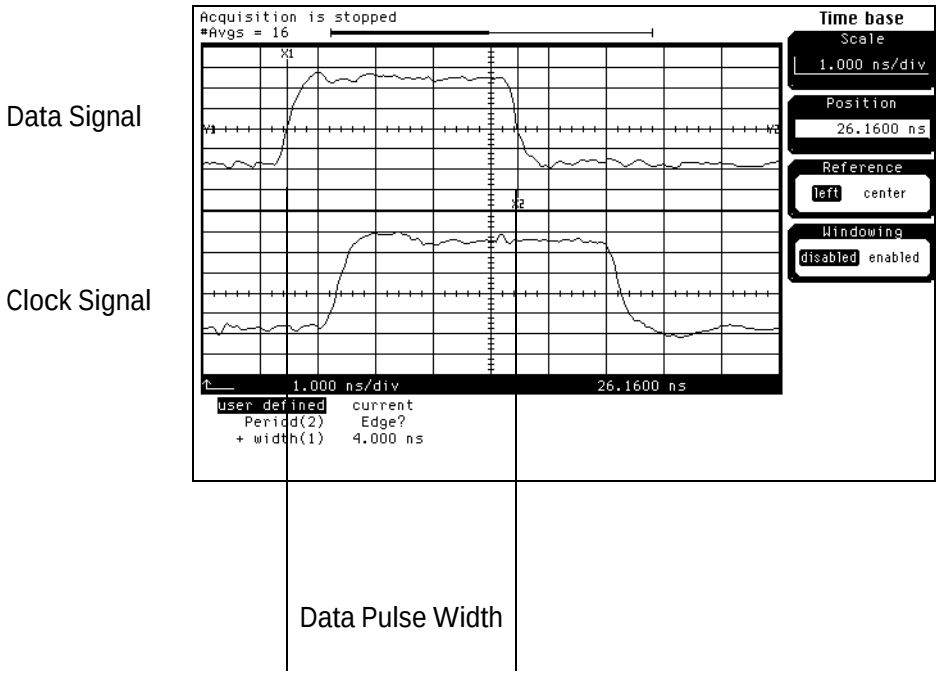
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

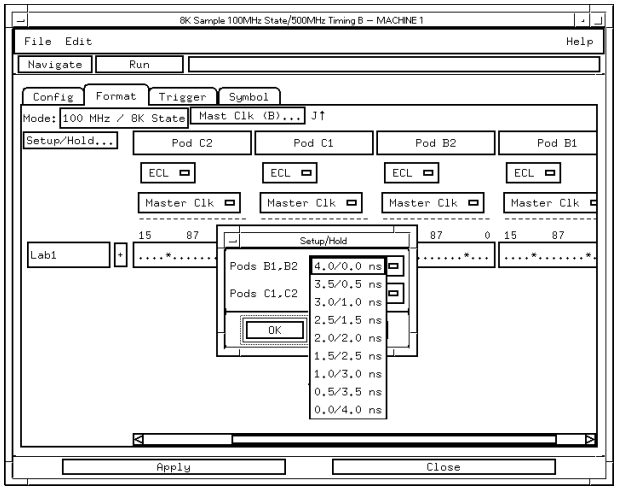
d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

- **a** In the MACHINE 1 setup window, select the Format tab.
- **b** Under the Format tab, select Setup/Hold.
- **c** In the Setup/Hold window, select the setup/hold field next to each pod pair, then select 4.0/0.0 ns. Repeat for all pods.



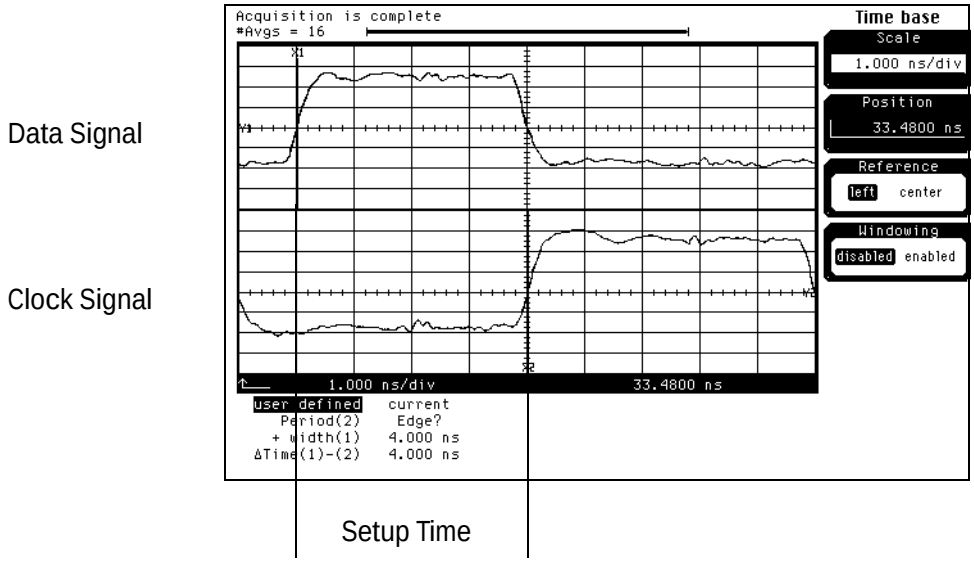
- **d** Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

- **a** On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.
- **b** In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.
- **c** On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

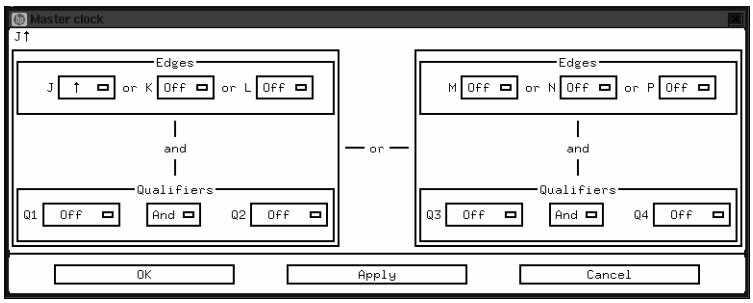
d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



4 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock ...

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Turn off all other clocks. The first time through this test, select the first clock and edge.



Clocks

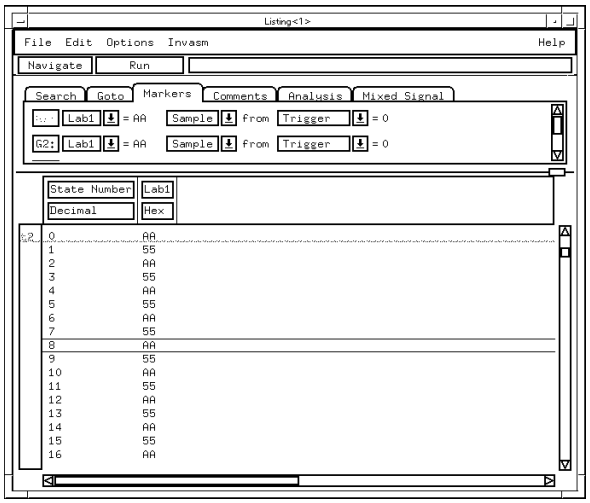
J↑	K↑	L↑	M↑	N↑	P↑

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

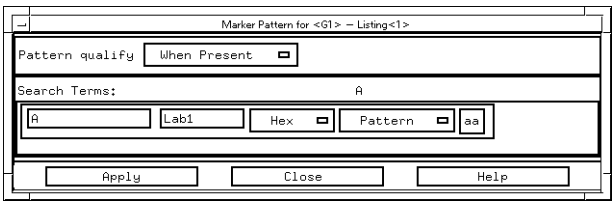
d Select OK.

5 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "AA" and "55".



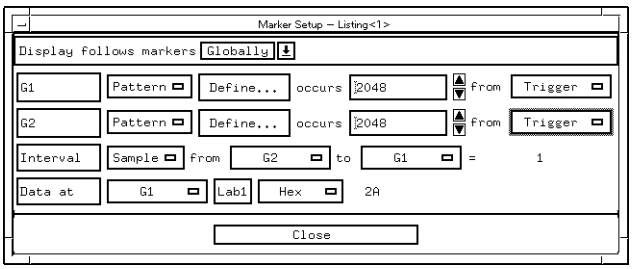
b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter "aa". Select Apply, then select Close.



c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter "55". Select Apply, then select Close.

d In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 2048.

e In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the "Pattern NOT found for marker…" error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock…

b Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

Performance Test Record

Performance Test Record

HEWLETT PACKARD	**HP 16710A, HP 16711A, or HP 16712A Logic Analyzer**
Serial No. _____	Work Order No._____
Recommended Test Interval - 2 Year/4000 hours	Date_____
Recommended next testing_____	Temperature_____

Test	**Settings**		**Results**	
Self-Tests			Pass/Fail	_____
Threshold Accuracy	±(100 mV + 3% of threshold setting)			
Pod 1			Limits	Measured
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____
Pod 2				
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____
Pod 3				
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____
Pod 4				
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____
Pod 5				
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____
Pod 6				
	ECL, ±139 mV	ECL VL	–1.439 V	_____
		ECL VH	–1.161 V	_____
	0 V, ±100 mV	0 V User VL	–100 mV	_____
		0 V User VH	+100 mV	_____

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition			Pass/Fail		Pass/Fail	
All Pods, Channel 3	Setup/Hold Time	4.0/0.0 ns	J↑ _____		J↓ _____	
			K↑ _____		K↓ _____	
			L↑ _____		L↓ _____	
			M↑ _____		M↓ _____	
			N↑ _____		N↓ _____	
			P↑ _____		P↓ _____	
	Setup/Hold Time	0.0/4.0 ns	J↑ _____		J↓ _____	
			K↑ _____		K↓ _____	
			L↑ _____		L↓ _____	
			M↑ _____		M↓ _____	
			N↑ _____		N↓ _____	
			P↑ _____		P↓ _____	
All pods, channel 11	Setup/Hold Time	4.0/0.0 ns	J↑ _____		J↓ _____	
			K↑ _____		K↓ _____	
			L↑ _____		L↓ _____	
			M↑ _____		M↓ _____	
			N↑ _____		N↓ _____	
			P↑ _____		P↓ _____	
	Setup/Hold Time	0.0/4.0 ns	J↑ _____		J↓ _____	
			K↑ _____		K↓ _____	
			L↑ _____		L↓ _____	
			M↑ _____		M↓ _____	
			N↑ _____		N↓ _____	
			P↑ _____		P↓ _____	

Test	Settings	Results
Multiple-clock, Multiple-edge Acquisition		Pass/Fail Pass/Fail
All Pods, Channel 3	Setup/Hold Time 5.0/0.0 ns	J↑+M↑+N↑ _____ J↓+M↓+N↓ _____ K↑+L↑+P↑ _____ K↓+L↓+P↓ _____
	Setup/Hold Time 0.0/5.0 ns	J↑+M↑+N↑ _____ J↓+M↓+N↓ _____ K↑+L↑+P↑ _____ K↓+L↓+P↓ _____
All Pods, Channel 11	Setup/Hold Time 5.0/0.0 ns	J↑+M↑+N↑ _____ J↓+M↓+N↓ _____ K↑+L↑+P↑ _____ K↓+L↓+P↓ _____
	Setup/Hold Time 0.0/5.0 ns	J↑+M↑+N↑ _____ J↓+M↓+N↓ _____ K↑+L↑+P↑ _____ K↓+L↓+P↓ _____
Single-Clock, Multiple-Edge Acquisition		Pass/Fail
All Pods, Channel 3	Setup/Hold Time 4.5/0.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____
	Setup/Hold Time 0.0/4.5 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____

Test	Settings		Results	
Single-Clock, Multiple-Edge Acquisition (continued)				Pass/Fail
All Pods, Channel 11	Setup/Hold Time	4.5/0.0 ns	J↕	_____
			K↕	_____
			L↕	_____
			M↕	_____
			N↕	_____
			P↕	_____
	Setup/Hold Time	0.0/4.5 ns	J↕	_____
			K↕	_____
			L↕	_____
			M↕	_____
			N↕	_____
			P↕	_____
Time Interval Accuracy				Pass/Fail
	Interval time from G1 to G2	25.592 - 25.608 µs		_____
Two-Card Test				Pass/Fail
	Setup/Hold Time	4.0/0.0 ns	J↑	_____
			K↑	_____
			L↑	_____
			M↑	_____
			N↑	_____
			P↑	_____

4

Calibrating

Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

Calibration Strategy

The HP 16710A/11A/12A logic analyzers do not require an operational accuracy calibration. To test the module against the module specifications, refer to "Testing Performance" in chapter 3.

5

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, a cable test, and a test for the auxiliary power supplied by the probe cable. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

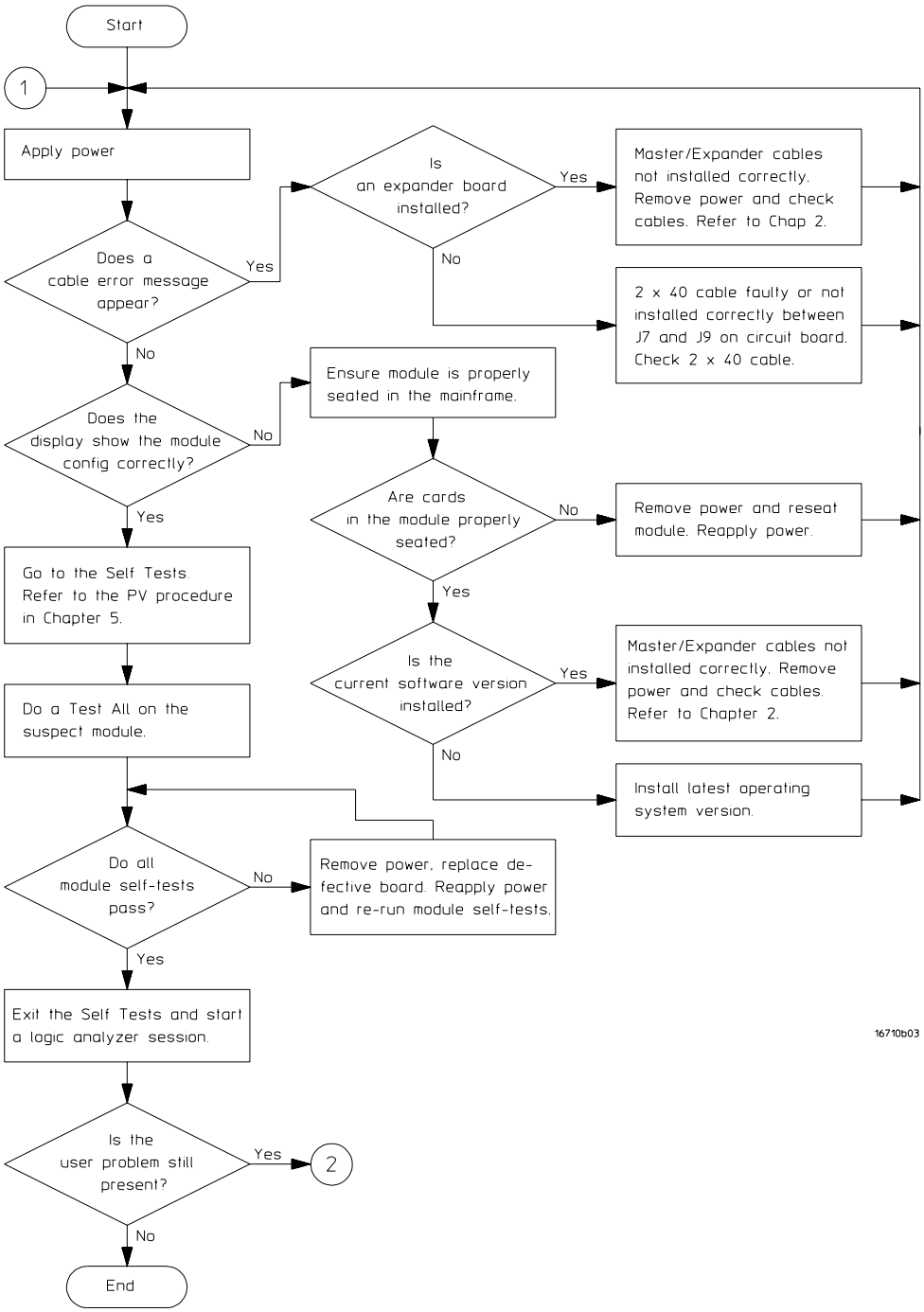
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

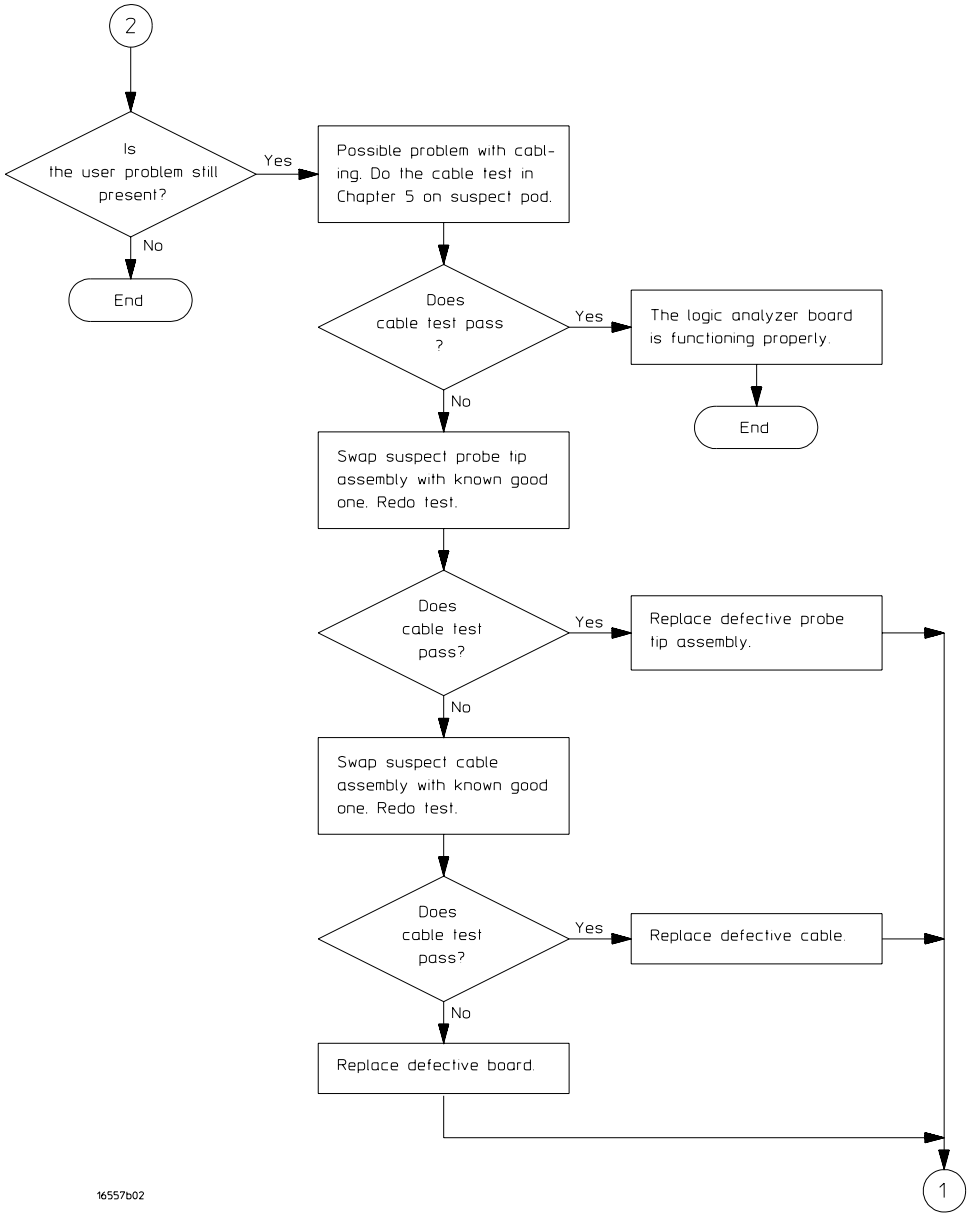
Mainframe Operating System

Before starting the troubleshooting on an HP 16710A/11A/12A, ensure that the required version of HP 16700A- or HP 16600A-series mainframe operating system is installed on the mainframe. The required operating system software versions are listed in "Mainframe and Operating System" in chapter 1. To check the operating system version number, open the System Administration window, click the Admin tab, then click About...

If the proper version is not loaded, obtain a copy of the updated operating system software and install it in the logic analyzer.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To run the self-tests

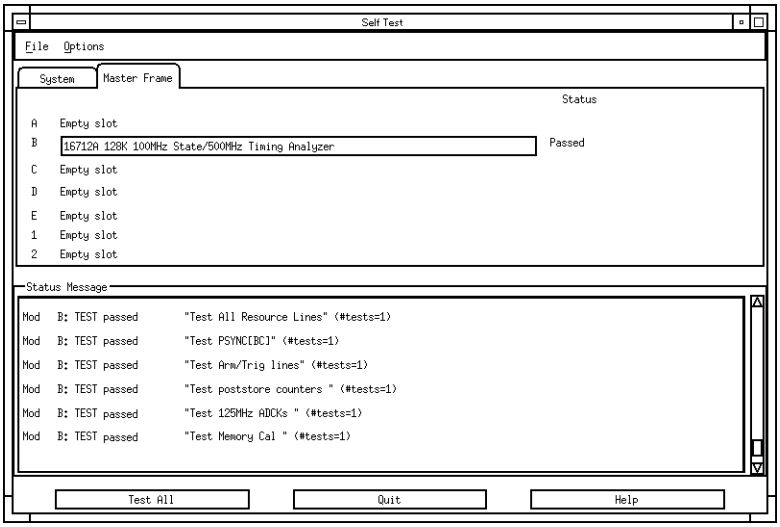
Self-tests identify the correct operation of major, functional subsystems of the module. You can run all self-tests without accessing the module. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the module.

To run the self-tests:

1. In the System window, select System Admin.
2. In the System Administration window, select the Admin tab, then select Self-Test. At the Test Query window, select Yes.

   The tests can be run individually, or all the tests can be run by selecting Test All at the bottom of the Self Test window. Note that if Test All is selected, system tests requiring user action will not be run. For more information, refer to Chapter 8 in the mainframe service manual.
3. In the Self Test window under the System tab, select System CPU Board.
4. Run the floppy drive test.
   a. In the Self Test: System CPU Board window, select Floppy Drive Test.
   b. Insert a DOS-formatted disk with 300 KB of available space in the mainframe floppy drive.
   c. In the Test Query window, select OK.

      The Test Query window instructs you to insert the disk into the drive. The other System CPU Board tests require similar user action to successfully run the test.
5. In the Self Test: System CPU Board window, select Close to close the window.
6. In the Self Test window, select PCI Board. Select Test All to run all PCI board tests.
7. In the Self Test window, select the Master Frame tab. Select the HP 16710A/11A/12A module to be tested, then select Test All to run all the module tests. The module test status should indicate PASSED (see screen on next page).



Refer to Chapter 8 in the mainframe service manual for more information on system tests that are not executed.

To exit the test system

To exit the test system

1. Select Close to close any module or system test windows.
2. In the Self Test window, select Quit.
3. In the session manager window, select Start Session on This Display to launch a new logic analyzer session.

To test the cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/ Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8133A Option 003
6x2 Test Connectors (Qty 4)		

1 If you have not already done so, do the procedure "To set up the test equipment and the logic analyzer" in Chapter 3.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Channel 1	Trigger
Mode: Int Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: 3.00 V Low: 0.00 V COMP: Disabled (LED Off)	Mode: Square Delay: 0.000 ns High: 3.00 V Low: 0.00 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

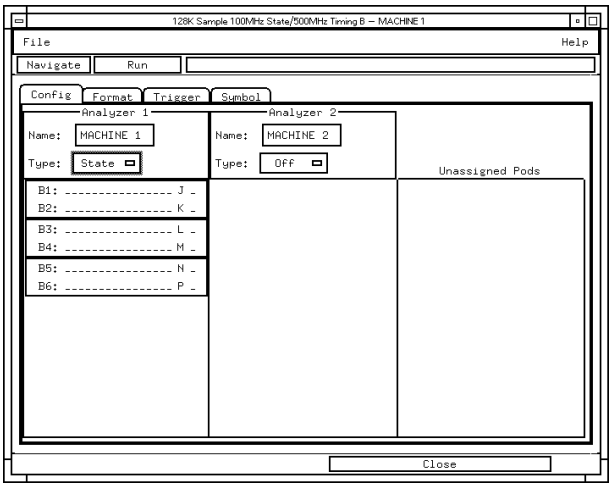
b Enable the pulse generator channel 1 and channel 2 outputs (LED off).

3 Set up the Configuration tab.

a In the MACHINE 1 window, select the Config tab.

b Ensure that they Type analyzer is set to State.

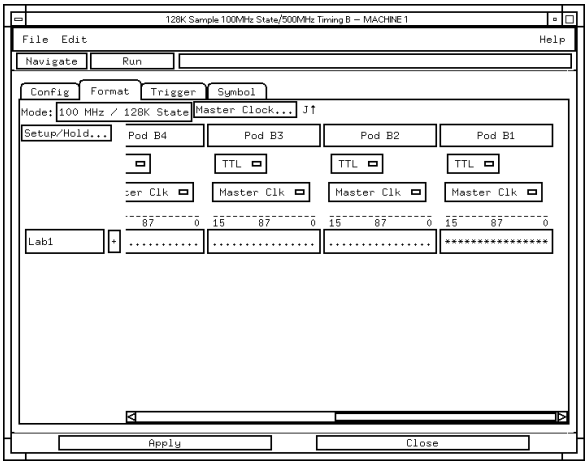
c Assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



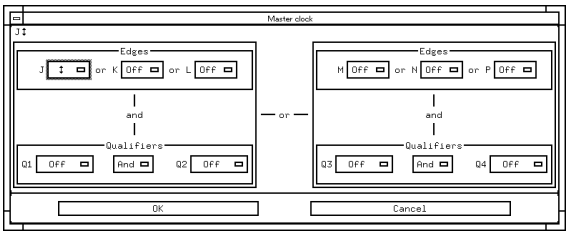
4 Set up the Format tab.

a In the MACHINE 1 setup window, select the Format tab.

b Select the field showing the channel assignments for the pod under test. In the pop-up menu, select the asterisk field to put asterisks in the channel positions, activating the channels. Select Done.



c Select Master Clock. In the Master Clock window, select a double edge for the J clock (J↕). Turn off the other clocks. Select Apply, then select OK to close the Master Clock window.



d Select Setup/Hold, then select 4.5/0.0 ns for the pod being tested. Select OK to close the Setup/Hold window.

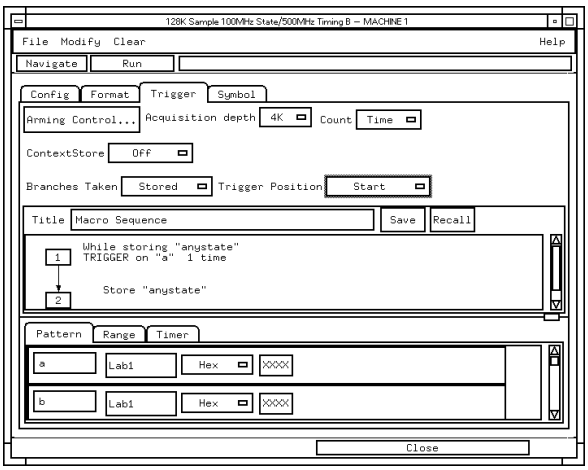
e Select the threshold field for the pod being tested, then select TTL.

5 Set up the Trigger tab.

a In the MACHINE 1 setup window, select the Trigger tab.

b Select the Acquisition Depth field, then select “4K”.

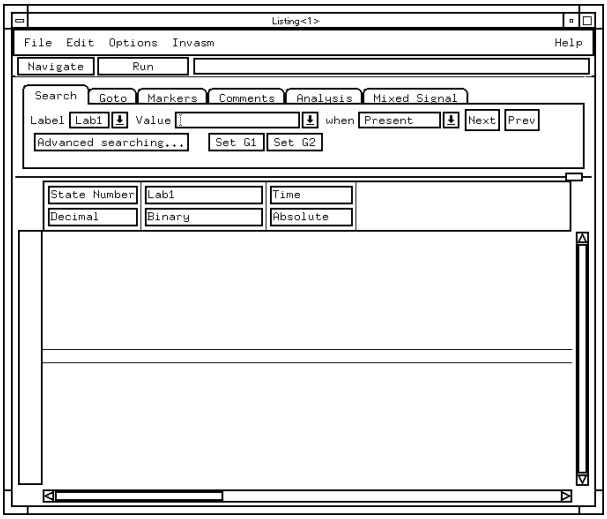
c Select the Trigger Position field, then select Start.



6 Set up the Listing window.

a In the MACHINE 1 Setup window, select Navigate, then select Slot n: MACHINE 1, then select Listing. A Listing window will open.

b Right click on the Hex field and change the Lab1 base to Binary.



7 Using four 6-by-2 test connectors, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, "Testing Performance."

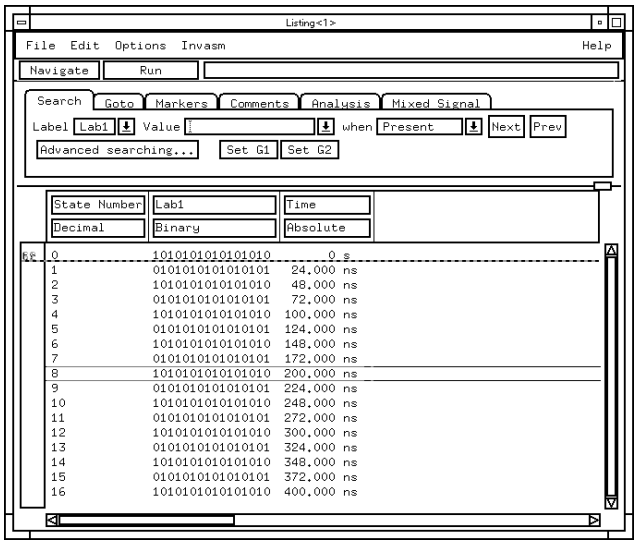
a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output.

c Connect the even-numbered channels of the upper byte of the pod under test and the J clock channel to the pulse generator channel 2 Output. J clock is located on Pod 1.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 Output.

8 On the logic analyzer, select Run. The listing should look similar to the figure below. Ignore any error messages dealing with the G1 and G2 markers.



9 If the listing looks like the figure, then the cable passed the test.

If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

Return to the troubleshooting flowchart.

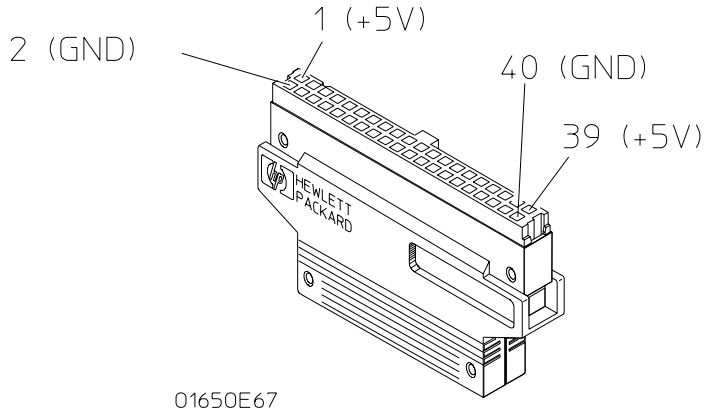
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection circuit. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Digital Multimeter	na	HP E2373A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.



6

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module. Also in this chapter are instructions for returning assemblies.

CAUTION Turn off the instrument before installing, removing, or replacing a module in the instrument.

Tools Required

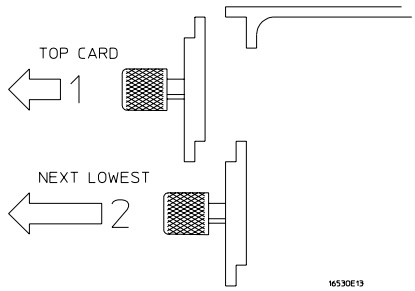
A T10 TORX screwdriver is required to remove screws connecting the probe cables and screws connecting the back panel.

To remove the module

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1. Remove power from the instrument.
   - **a** Exit all logic analysis sessions. In the session manager, select Shutdown.
   - **b** At the query, select Power Down.
   - **c** When the "OK to power down" message appears, turn the instrument off.
   - **d** Disconnect the power cord.
2. Loosen the thumb screws.

   Starting from the top, loosen the thumb screws on the filler panels and cards located above the module and the thumb screws of the module.



3. Starting from the top, pull the cards and filler panels located above the module half-way out.
4. If the module consists of a single card, pull the card completely out.

   If the module consists of multiple cards, pull all cards completely out.
5. Push all other cards into the card cage, but not completely in.

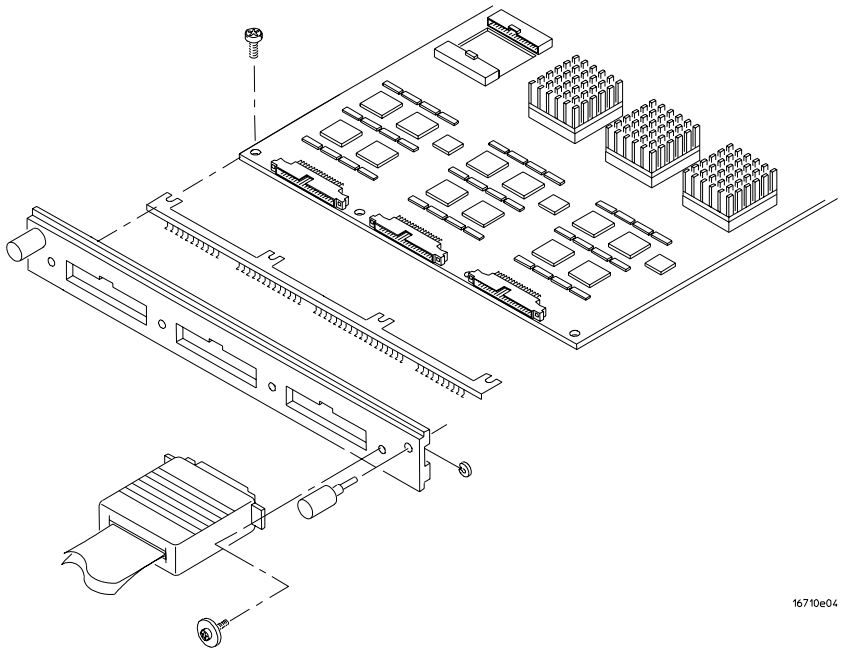
   This is to get them out of the way for removing and replacing the module.
6. If the module consist of a single card, replace the faulty card.

   If the module consists of two cards, remove the 2x40 cable from J8 of the master card. Remove the 2x25 cables from J5 and J6 from both cards. Remove the faulty card from the module.

To replace the circuit board

1. Remove the three screws connecting the probe cables to the back panel, then disconnect the probe cables.
2. Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.
3. Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 80-pin ribbon cable is connected between J7 and J9.
4. Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.
5. Connect the probe cables, then install three screws to connect the cables to the back panel.

CAUTION If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.



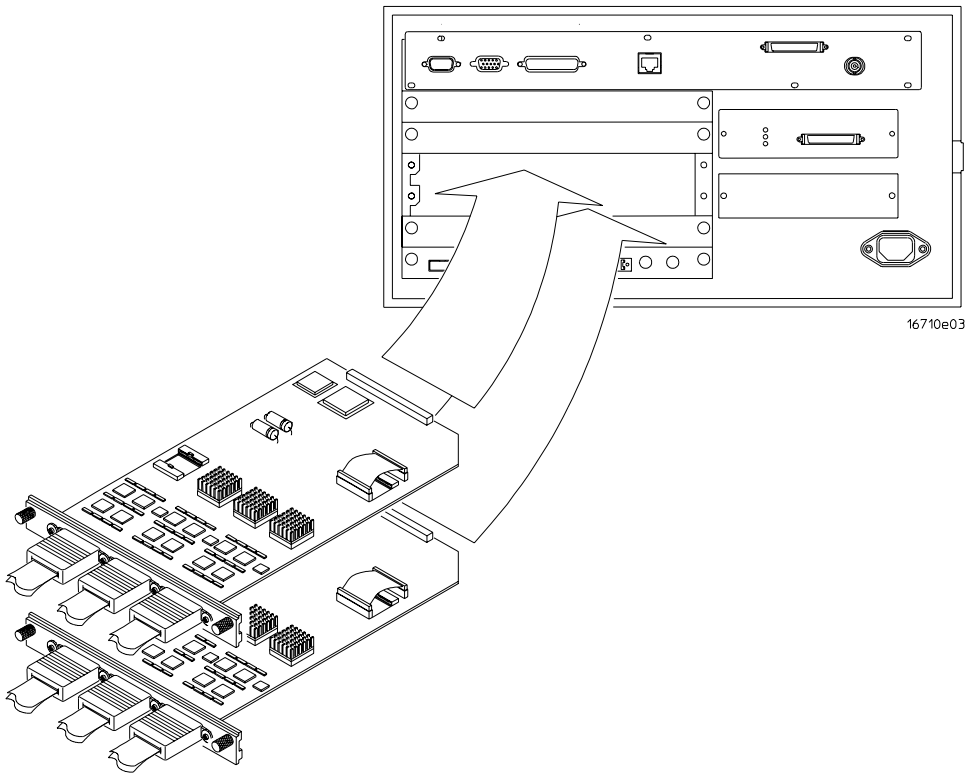
To replace the module

1. If the module consists of one card, go to step 2.

   If the module consists of two cards, connect the cables together in a master/expander configuration. Follow the procedure "To configure a two-card module" in chapter 2.

2 Slide the cards above the slots for the module about halfway out of the mainframe.

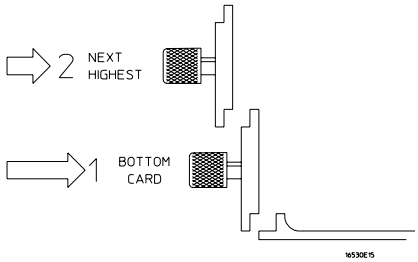
3 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



4 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 6.

5 Position all cards and filler panels so that the endplates overlap.



6 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

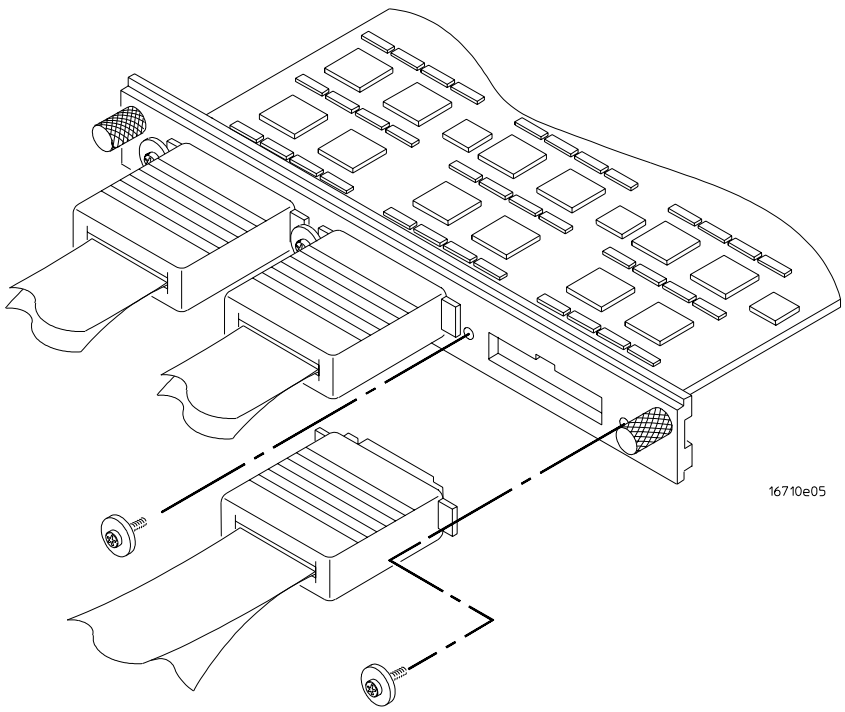
CAUTION Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To replace the probe cable

1. Remove power from the instrument.
   - **a** Exit all logic analysis sessions. In the session manager, select Shutdown.
   - **b** At the query, select Power Down.
   - **c** When the "OK to power down" message appears, turn the instrument off.
   - **d** Disconnect the power cord.
2. Remove the screws that hold the probe cable to the rear panel of the module.
3. Remove the faulty probe cable from the connector and install the replacement cable.
4. Install the label on the new probe.

   If you order a new probe cable, you will need to order new labels. Probe cables shipped with the module are labeled. Probe cables shipped separately are not labeled. Refer to chapter 7, "Replaceable Parts," for the part numbers and ordering information.
5. Install the screws connecting the probe cable to the rear panel of the module.

CAUTION If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.



To return assemblies

Before shipping the module to Hewlett-Packard, contact your nearest Hewlett-Packard Sales Office for additional details. In the U.S., call 1-800-403-0801.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the module.

Only return accessories to Hewlett-Packard if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an HP sales office.

CAUTION For protection against electrostatic discharge, package the module in electrostatic material.

4 Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Hewlett-Packard Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Hewlett-Packard Sales Office.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the HP Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Hewlett-Packard Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Hewlett-Packard to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Hewlett-Packard Sales Office. Addresses and telephone numbers are located in a separate document shipped with the *HP 16700-series Logic Analysis System Service Manual*.

Exchange Assemblies

Some assemblies are part of an exchange program with Hewlett-Packard.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Hewlett-Packard.

After you receive the exchange assembly, return the defective assembly to Hewlett-Packard. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Hewlett-Packard will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Hewlett-Packard Sales Office for information.

See Also

"To return assemblies," page 6-8.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator
- Hewlett-Packard part number
- Total quantity included with the module (Qty)
- Description of the part

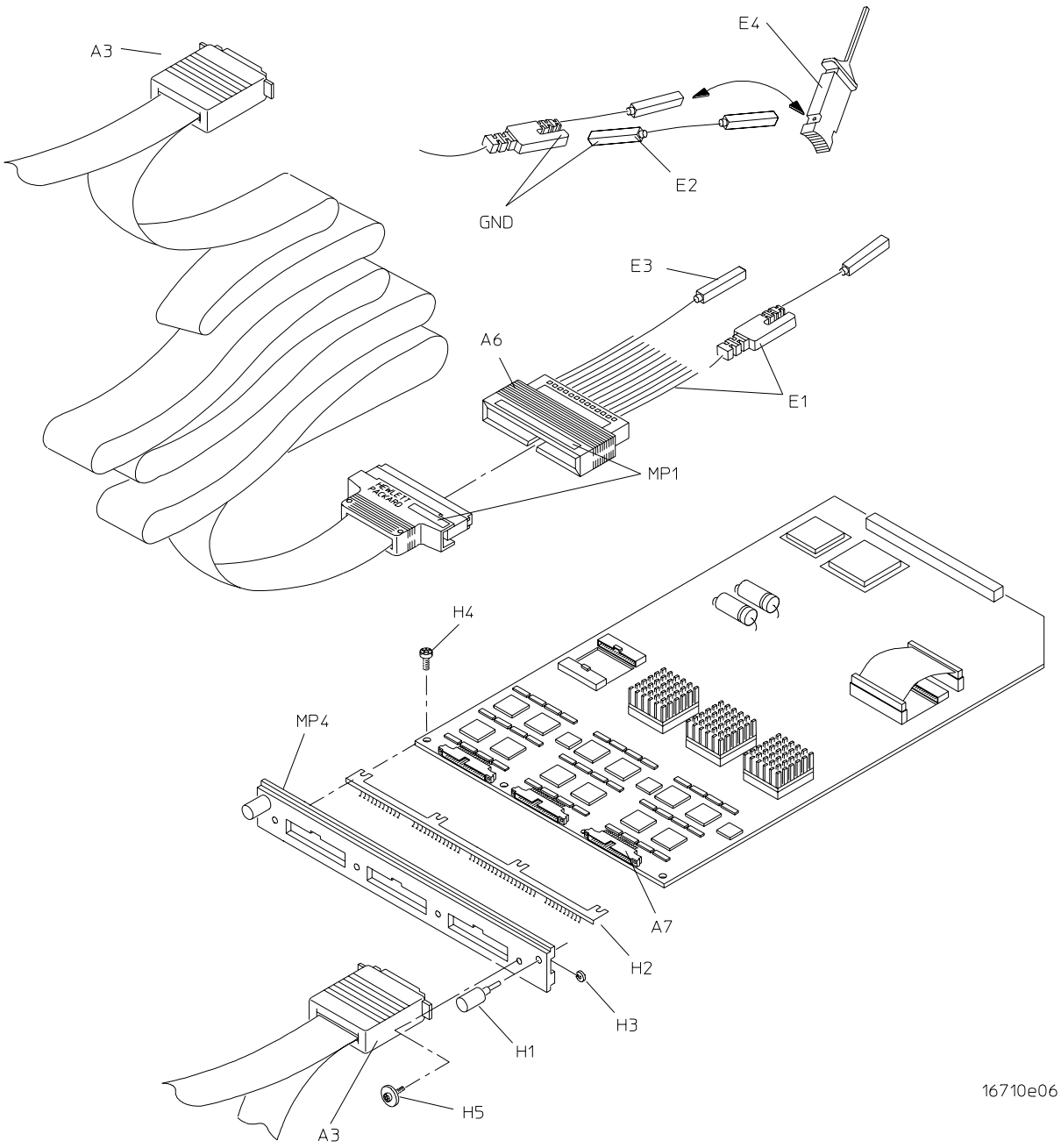
Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
	16710-69501	1	Exchange Board Assembly (HP 16710A)
	16710-69502	1	Exchange Board Assembly (HP 16711A)
	16710-69504	1	Exchange Board Assembly (HP 16712A)
A1	16710-66501	1	Board Assembly (HP 16710A)
A1	16711-66502	1	Board Assembly (HP 16711A)
A1	16712-66504	1	Board Assembly (HP 16712A)
A2	16710-61601	1	Interconnect Cable 80-pin
A3	16557-61601	3	Probe Cable
A3	16710-61602	3	Probe Cable, Shielded
A4	16555-61601	1	Master/Expander Cable 50-pin
A6	01650-61608	6	Probe Tip Assembly
A7	1252-4181	3	Probe Cable Socket - 50 pin
A8	16542-61607	1	Double Probe Adapter
E1	5959-9333	1	Probe Leads Replace (5 Per Package)
E2	5959-9334	6	Probe Ground Replace (5 Per Package)
E3	5959-9335	0	Pod Ground Replace (2 Per Package)
E4	5090-4356	6	Grabber Kit Assembly (20 Grabbers Per Package)
H1	16500-22401	2	Panel Screw
H2	16550-29101	1	Ground Spring
H3	0510-0684	2	Retaining Ring
H4	0515-0430	4	MS M3.0X0.5X6MM PH T10 (Endplate Screw)
H5	0515-2306	4	Screw Sems M3 X 0.5X10mm (Cable Retaining Screw)
MP1	01650-94312	1	Label-Probe and Cable
MP4	16550-40501	1	Module Panel
MP6	16710-94301	1	Label-ID (HP 16710A)
MP6	16711-94301	1	Label-ID (HP 16711A)
MP6	16712-94301	1	Label-ID (HP 16712A)

Exploded View



Exploded view of the HP 16710A/11A/12A logic analyzer

8

Theory of Operation

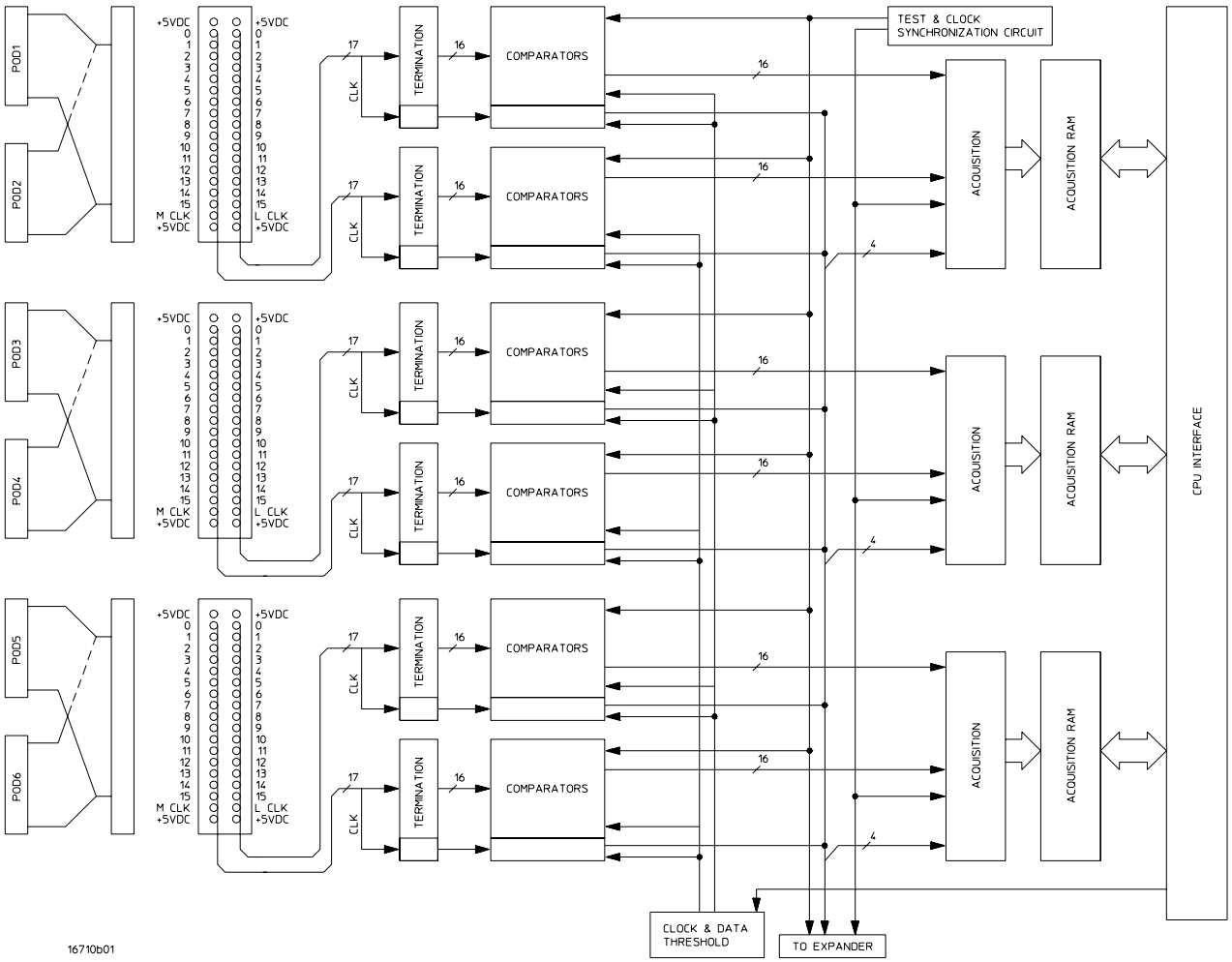
Theory of Operation

This chapter presents the theory of operation for the logic analyzer module and describes the self-tests. The information in this chapter is to help you understand how the module operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory of operation is divided into two parts: theory for the logic analyzer used as a single-card module or as a master card in a two-card module, and theory for the logic analyzer used as an expander card in a two-card module. A block diagram is shown before each theory.

The HP 16710A/11A/12A logic analyzer



Probing. The probing system consists of a tip network, a probe cable, and terminations which reside on the analyzer card. Each probe cable is made up of two woven cables, each one carrying 16 data channels and 1 clock/data channel. The four clock/data channels on each logic analyzer plus the 64 data channels on each logic analyzer card results in a maximum of 68 available data acquisition channels for each card.

Each channel of the probing system has its own ground. In addition the pod has a single ground. For applications where more than three channels are used and signal risetimes are less than 3 ns, individual channel grounds should be used.

The probe tip networks comprise a series of resistors (250 Ohm) connected to a parallel combination of a 90 KΩ resistor and a 8.5 pF capacitor. The parallel 90 KΩ and 8.5 pF capacitor along with the lossy cable and terminations form a divide-by-ten probe system. The 250-Ohm tip resistor is used to buffer (or raise the impedance of) the 8.5 pF capacitor that is in series with the cable capacitance.

Comparators. Two 9-channel comparators per pod interpret the incoming data and clock signals as either high or low, depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparators has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparators. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, the operating system software can test all data and clock channel pipelines on the circuit board through the comparator.

Acquisition. Each acquisition circuit is made up of a single acquisition IC. Each acquisition IC is a 34-channel state/timing logic analyzer. Three acquisition ICs are included on every logic analyzer card for a total of 96 data channels and 6 clock/data channels. All of the sequencing, storage qualification, pattern/range recognition and event counting functions are performed by the acquisition IC.

Also, the acquisition ICs perform master clocking functions. All six state acquisition clocks are sent to each acquisition IC, and the acquisition ICs generate their own sample clocks. Every time the user selects RUN, the acquisition ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays in the acquisition ICs to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase 125-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (125 MHz and faster), the four-phase 125-MHz clock signal determines the sample period. For slower sample rates, one of the two acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The sample clock is then sent to the other acquisition ICs.

Acquisition RAM. The acquisition RAM is external to the acquisition IC. The acquisition RAM consists of three RAM ICs (one RAM IC per pod pair). A memory management circuit controls RAM addressing during an acquisition run and during data upload to the mainframe CPU.

Test and Clock Synchronization Circuit. ECLinPS (ECL in pico seconds) ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification (self-tests). The test patterns are propagated across all data and clock channels and read by the acquisition ICs to verify that the data and clock pipelines are operating correctly.

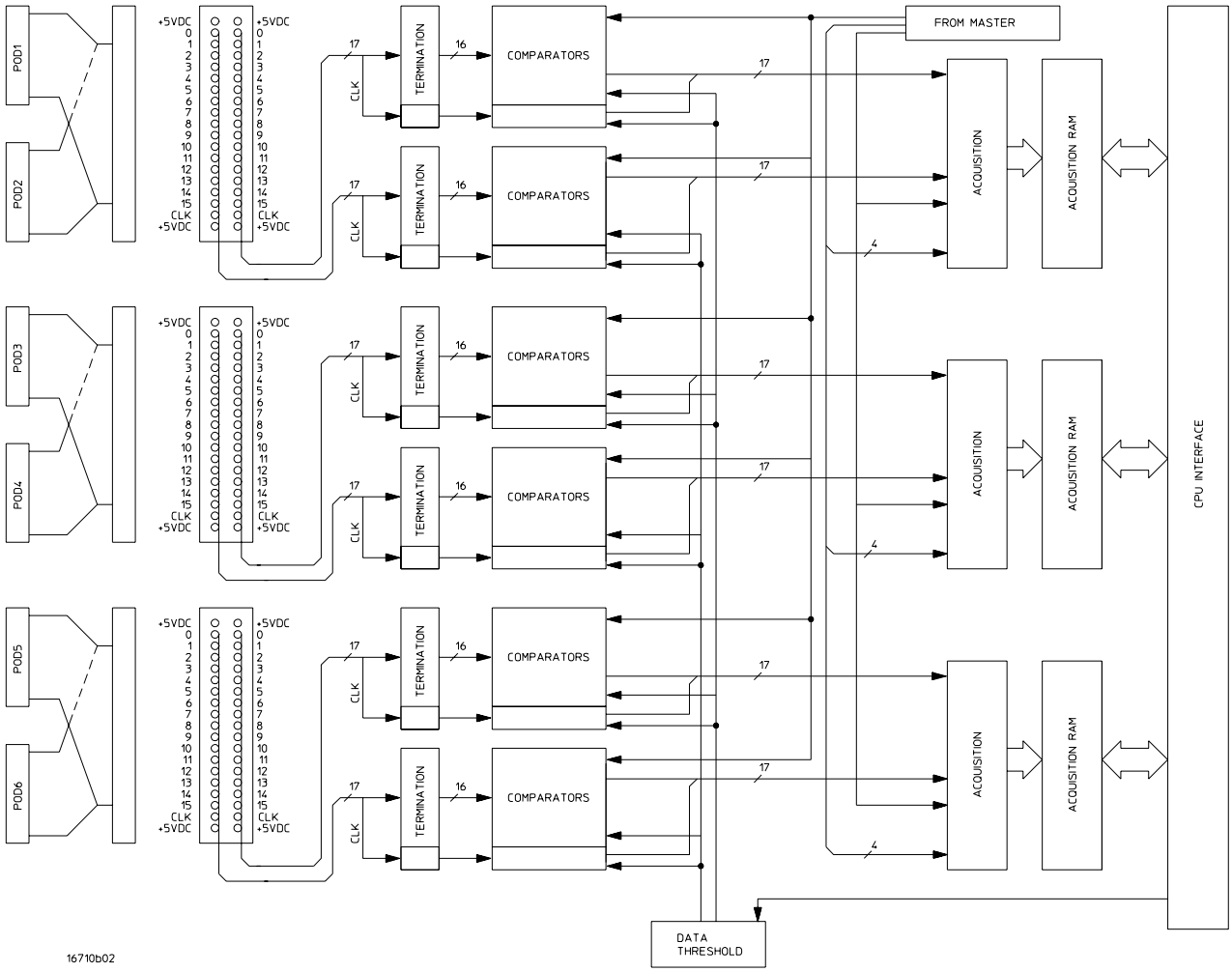
Also, the Test and Clock Synchronization Circuit generates a four-phase 125-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. At fast sample rates, the synchronizing signal keeps the internal clocking of the individual acquisition ICs locked in step with the other acquisition ICs in the module. At slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by both acquisition ICs.

Clock and Data Threshold. The threshold circuit includes a precision DAC and precision op amp drivers. Each of the output channels of the DAC is individually programmable which allows the user to set the thresholds of the individual pods. The 16 data channels and the clock/data channel of each pod are all set to the same threshold voltage.

CPU Interface. The CPU interface is a programmable logic device that converts the bus signals generated by the microprocessor on the mainframe CPU card into control signals for the logic analyzer card. All functions of the state and timing card can be controlled from the backplane of the mainframe system including storage qualification, sequencing, assigning clocks and qualifiers, RUN and STOP, and thresholds. Data transfer between the logic analyzer card and the mainframe CPU card is also accomplished through the CPU interface.

+5 VDC supply. The +5 VDC supply circuit supplies power to active logic analyzer accessories such as analysis probes. Thermistors on the +5 VDC supply lines and on the ground return line protect the logic analyzer and the active accessory from overcurrent conditions. When an overcurrent condition is sensed, the thermistors create an open that shuts off the current from the +5 VDC supply. After a reset time of approximately 1 minute, the thermistor closes the circuit and makes the supply current available.

The HP 16710A/11A/12A logic analyzer as an expander



Two HP 16710A/11A/12A logic analyzers can be connected together in a two-card master/expander configuration. All of the functions of the logic analyzer configured as a master are retained by the logic analyzer configured as an expander with a few exceptions. As a master and expander multi-card logic analyzer module, most of the supporting circuitry on the expander configured card is disabled to allow both the master and expander cards to operate together as one 204-channel module with no compromise in functionality. The same signals that drive the acquisition ICs on the master configured card also drive the acquisition ICs on the expander configured card.

Acquisition. The six clocks sent to the master card are also sent to the acquisition ICs on the expander card. The acquisition ICs on the expander card individually generate their own sample clock for the state acquisition mode. For timing acquisition mode, the master card also passes the synchronization signal to the expander cards.

The six clock/data lines on the expander card pods are not available for either state mode clocking or state clock qualification. However, the six clock/data lines are still available as data channels.

Test and Clock Synchronization Circuit. The signals generated by the Test and Clock Synchronization Circuit of the master card are sent to the expander card. The Test and Clock Synchronization Circuit on the expander card is disabled to allow the master-configured card to drive the expander-configured card. The functionality of the Test and Clock Synchronization Circuit remains the same, but the circuit drives up to four more acquisition ICs and up to eight more comparator test inputs.

Threshold. The thresholds of each of the expander card pods are individually programmable, as with the master card pods. The threshold of the data and clock/data channels of each pod is set to the same threshold voltage. The clock/data channel on each pod of the expander card is available only as a data channel.

Self-Tests Description

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Write/Read the EPLD. A programmable logic device (PLD) is utilized as an interface between the logic analysis system backplane and the logic analyzer module. This test verifies that data can be reliably transferred from the mainframe backplane to the logic analyzer module. Passing the Write/Read the EPLD test implies that the PLD is not corrupted and that data can be passed between the logic analyzer module and the mainframe backplane.

Load FPGA. A Field Programmable Gate Array (FPGA) contains all the logic required to manage and control the logic analyzer module. While the PLD provides the hardware interface to the backplane, the FPGA converts the backplane signals into module control and configuration signals. The Load FPGA test loads an image file into the FPGA device while the FPGA itself monitors any load failures. If any load failure occurs, the FPGA will assert an error flag and the test will fail. Passing the Load FPGA test implies that the FPGA is operating properly and will load and store a configuration image file.

Test Cable Dtct Bits. During the mainframe power-up routine at Logic Analysis System load, the mainframe polls the module configuration as installed in the mainframe card cage. During this polling, the mainframe will verify that the logic analyzer module is correctly configured by asserting a cable detect signal through the master/expander cables. The Test Cable Dtct Bits test the cable detect signal. Passing the Test Cable Dtct Bits test implies that the mainframe and module will recognize misconfigured master/expander cabling.

Write/Read Board-level Regs. The Write/Read Board-level Regs test verifies the correct operation of the registers on the logic analyzer module. Passing the Write/Read Board-level Regs test implies that all bits of each board-level register can store both a logic "1" and a logic "0".

Write/Read Chip(n) Regs. The Write/Read Chip(n) Regs verifies the integrity of the 8-bit data bus that configures each of the three acquisition ICs (plus three acquisition ICs on an expander board). The test also verifies the correct operation of the registers that reside on each IC. Passing the Write/Read Chip(n) Regs test implies that each acquisition IC can be properly configured for each acquisition mode.

Test ZCal. The ZCal circuit optimally sets the output impedance of the acquisition IC to match the input impedance of the acquisition memory control circuit. Consequently the transmission lines to the memory control circuit are properly terminated. The Test ZCal test attempts to optimize the output impedance of the acquisition IC to the acquisition memory control circuit. Passing the Test ZCal test implies that the signal integrity between the acquisition IC and the acquisition memory control circuit is optimum so the acquisition memory will properly step with each acquisition.

Test MACS. The functionality of the memory address counters (MACS, one per acquisition IC) is tested. Passing the Test MACS test implies that the memory address counters will properly respond to the acquisition IC and increment the memory with each acquisition. This test is done in preparation for the memory test performed later.

Test MAC Records. The Test MAC Records verifies context-store capability of the acquisition memory system. Passing the Test MAC Records test implies that the memory address counters can properly configure and store context records.

Test State Clocks. The Test State Clocks test verifies all the state clock circuitry on the acquisition ICs including delay lines, edge detect, qualifiers and combiners. Passing the Test State Clocks test implies that the state clock circuitry on board each acquisition IC can be properly configured and is functional.

Test Timing Clocks. The Test Timing Clocks test first verifies the functionality of the delay line in the 125-MHz clock circuit in the acquisition ICs. The clock divider is then tested. Passing the Test Timing Clocks test implies that the timing clock circuitry is operating properly.

Chip Calibration. The Chip Calibration test verifies the correct operational accuracy calibration of each acquisition IC in a number of test configurations. This operational accuracy calibration optimizes the channel-to-channel skew of the data lines with respect to the clock signal. Passing the Chip Calibration test implies that each acquisition IC will properly zero the data lines to minimize skew.

Test Mems for Stuck Datalines. The Test Mems for Stuck Datalines verifies that acquisition memory is operational. A logic "0" is first stored in all accessible acquisition memory locations and then read. Then a logic "1" is stored and read. Passing the Test Mems for Stuck Datalines implies that acquisition memory is operating as expected, and each memory location bit can store a logic "0" or a logic "1".

Test Mems for Crossed Datalines. A walking "1" pattern and a walking "0" pattern is stored in the base memory address to verify that data lines in the acquisition memory are not shorted together. Passing the Test Mems for Crossed Datalines test implies that no acquisition memory data lines are shorted together.

Test for Faulty adrs lines. The Test for Faulty adrs lines test verifies that the acquisition memory address lines are not shorted together. Passing the Test for Faulty adrs lines test implies that none of the address lines are stuck, and that all accessible memory locations can be written to and read from.

Final Mems Test. The Final Mems Test exercises both the acquisition memory and the tag counter for each acquisition IC. The tag counter is incremented and a test pattern is written to a memory address in the acquisition memory. When the acquisition memory is full, the test pattern is read and compared with a known value. Passing the Final Mems Test implies that the acquisition memory for each acquisition IC is operating properly and can store measurement data.

Test Record Flags. The Test Record Flags exercise flag signals to acquisition memory. Passing the Test Record Flags test implies that the memory can be properly managed during an acquisition.

Test Timebase. The Test Timebase test verifies the 125-MHz timebase clock on the logic analyzer module. The operation of the clock is first tested, then the precision of the frequency is verified to within defined limits.

Test Thresholds/Comparators. The Test Thresholds/Comparators test verifies the correct operation of the comparators. First the comparators are swept through their operating range, and the floating "1" or "0" is read on each data line. If a floating value is not as expected on any channel, then the channel is reported. Passing the Test Thresholds/Comparators test implies that the logic analyzer front end is operating properly and all channels are capable of passing data to the acquisition ICs.

Write/Read I2C Chip. The Intra Integrated IC (I2C) bus manages the communication between the acquisition ICs. This bus is controlled by a single I2C Master control chip. The Write/Read I2C Chip test verifies the ability to write/read to the I2C Master control chip. Passing the Write/Read I2C Chip implies that the I2C Master control chip is configurable, and that communications between the acquisition ICs can be properly managed.

Test All Resource Lines. The pattern, range, edge, and glitch recognizers are tested and verified for all possible resource permutations and conditions. Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. In a two-card module, this test can only be run from the master card.

Test PSYNC[BC]. The PSYNC signals are used to synchronize acquisition ICs configured to the same logic analyzer machine. The PSYNCA signal has been utilized during the Self Tests. Consequently the PSYNCB and PSYNCC signals must be verified. Passing the Test PSYNC[BC] test implies that all acquisition ICs assigned to either Machine 1 or Machine 2 will acquire data together on each state or timing clock. In a two-card module, this test can only be run from the master card.

Test Arm/Trig lines. The Test Arm/Trig lines test verifies the operation of the Arm and Trigger lines between the logic analyzer Machine 1 and Machine 2. Passing the Test Arm/Trig lines test implies that either of the logic analyzer machines can arm or trigger the other machine. In a two-card module, this test can only be run from the master card.

Test poststore counters. The Test poststore counters test verifies the correct operation of the poststore counter on the acquisition IC. Passing this test implies that the poststore counter is operating correctly and can properly signal the end of an acquisition.

Test 125MHz ADCKs. The memory address counters (MACS) are run at full speed dual bank storage mode for 500-MHz timing acquisition (half-channel mode). Passing the Test 125MHz ADCKs test implies that acquisition memory management is operational in half-channel acquisition modes.

Test Memory Cal. The operational accuracy calibration for both the address and data buses of acquisition memory is done to ensure the address, memory, and data rates can be aligned to ensure acquisition data is properly stored. Passing the Test Memory Cal test implies that the address rate, rate of memory increment, and the data values can be properly synchronized and the data properly stored.

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About this edition

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